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Multiplier Based and Canonical Signed Digit Based VLSI Architecture for Discrete Wavelet Transformation

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ABSTRACT

THE DISCRETE wavelet transform (DWT) is a multi resolution analysis tool with excellent characteristics in the time and frequency domains. Through the DWT, signals can be decomposed into different sub-bands with both time and frequency information. The coding efficiency and the quality of image restoration with the DWT are higher than those with the traditional discrete cosine transform. Moreover, it is easy to obtain a high compression ratio. As a result, the DWT is widely used in signal processing and image compression.

Discrete Wavelet Transform (DWT) has been successfully used in the wide range of application including numerical analysis, signal analysis, image & video coding. It is found that DWT is two channels FIR filter computation one is low-pass FIR filter and other is high-pass FIR filter. Low-pass sub band is further decomposed to achieve multilevel DWT computation but in certain application like medical, images, fingerprint where both the low and high-pass sub band is required. For multilevel computation, this can be achieved by using discrete wavelet packet transform (DWPT).

Here we try to determine the best solution for optimizing the speed and area of the design. We calculate area and power for proposed design and compare to previous approach.

Keywords-- Discrete wavelet transform, Multipliers and canonical signed digit, VLSI

1. Introduction

Discrete Wavelet Transform (DWT) has been successfully used in the wide range of application including numerical analysis, signal analysis, image & video coding, pattern recognition, statistics and physics.

Silicon-area, speed, power consumption and design cost are the general parameters that are taken care while designing VLSI architecture, DSP system and high performance system. At this time, low-complexity design is the most important parameter of the VLSI architecture. However, in recent years, power is being given more importance as area and speed due to phenomenal growth of portable and wireless handheld multimedia devices. The power consumption is the most critical design concern for these devices. In this paper, efficient VLSI architecture for discrete wavelet packet transform (DWPT) is introduced in the multiplier based (MB) architecture and canonic signed digit based (CSDB) architecture. The Efficient VLSI architecture for DWPT is proposed for high speed on-line applications. With this architecture speed of the sample increases, occupied area as well as power consumption of the architecture reduces. Here we try to determine the best solution to this problem by Canonic Signed Digit (CSD) based architecture.

2. Related Work

Firstly, Zhang et. al. proposed achieved an efficient folded architecture (EFA) with low hardware complexity. However, its critical path delay is $Tm + Ta$, where Tm and Ta are the delay of a multiplier and an adder, respectively, and the computation time of EFA is quite long. Through optimizing the lifting scheme a pipelined architecture to reduce the critical path to one multiplier and limit the size of the temporal buffer to $4N$, but it has one input and one output and cannot achieve high processing speed. A limitation of the structure is that, it uses only one buffer when carrying out the transformation it has one input and one output and cannot achieve high processing speed.

After that Wu.et al. proposed a programmable one-dimensional discrete wavelet packet transform processor. Compared with existing architectures, the proposed processor can carry out both wave transforms and wavelet packet transforms, and is suitable for high-tap filters and high decomposition levels. It is small, and is especially suitable for on-chip or single-chip implementation. A limitation of the structure is that, it uses only one buffer when carrying out the transformation. Each time we obtain two new coefficients (one a high-pass coefficient, the other a low-pass coefficient),

we have to store them in the same buffer at the positions where the two corresponding original pieces of data to be abandoned are located. Therefore, the order of the coefficients is not as clear as it would be in a software implementation. It is found that the interval between two adjacent coefficients in the same frequency band is $2^J$when the decomposition level is J,and the position of the first coefficient in a frequency band equals the binary bit-reverse of the index of that band.

Trenas et al. proposed an architecture for wavelet packet based speech enhancement for hearing aids. Wavelet packet transform has been applied in order to compensate the speech signal to improve the intelligibility for a common hearing impairment known as recruitment of loudness, a sensor neural hearing loss of cochlear origin. In this paper presents DWPT is implemented using convolution based approach. In this paper up to 3-level architecture for DWPT is implemented using 8-multipliers, 6-adders and the memory storage size is N. In compare with the Wu et al.,architecture the memory is reduced in N-times.

Trenaset al., paper is based on configurable architecture for wavelet packet transform. By applying a folded and internally pipelined wavelet (PE) at each level, this new architecture can perform the real-time processing with a high throughput of N/2-cycle for N-point DWPT. In this paper, up to 3-level architecture for WPT in 8-multiplier and 6-adder are used and the memory storage size is reduced in the Trenas et. al. This architecture comprises of (4(N-1)) memory storage size and N processing cycles. So that can achieve significant reduction in both die area and power dissipation.

Later on Mohsen et al. proposed architecture of a wavelet packet transforms using parallel filters. This architecture increases the speed of the wavelet packet transforms. In this design, a word-serial architecture able to compute a complete wavelet packet transform (WPT) binary tree in an on-line fashion, and easily configurable in order to compute any required WPT sub tree is proposed. In this paper, based on the word-serial pipelined architecture and parallel filter processing with high-pass and low-pass filters, a new architecture for the wavelet packet transform is introduced. Using two filters, one high-pass and one low-pass concurrently, divided the latency of the memories to half. This architecture reduces the area and power consumption but increases the computation time by factor of four.

In this paper, the author Comparing DWPT with DWT and find the difference that, in DWT the range of operation is halved with a change in decomposition level J, while in DWPT the range of operation is always the whole frame. So, as the operation range halved with the increase in decomposition level, the DWPT is used to decrease the area of chip as well as to power consumption with high speed applications.

3. Algorithm & Implementation

In Figure, the original signal X[n] has N-sample points, is passed through 1×2 demultiplier. When select line is 0 then we get even sample and when select line is 1 then we get odd sample.

In Figure, at the third decomposition level, the time period is doubled and frequency will be half, and the output of CSD based low-pass and high-pass filter is passed through a register unit. Now the output of register unit is passed through mux. When the select line is 00, we get CSD based low-pass filter output Y_{LL}, the select line is 01, we get Y_{LH}, the select line is 10, we get Y_{HL} and the select line is 11 we getY_{HH}. Now finally we have passed mux output through CSD based low pass filter and high pass filter we get Y_{LLL},Y_{LHL}, Y_{HLL}, Y_{HHL} and Y_{LLH}, Y_{LHH}, Y_{HLH}, Y_{HHH}.

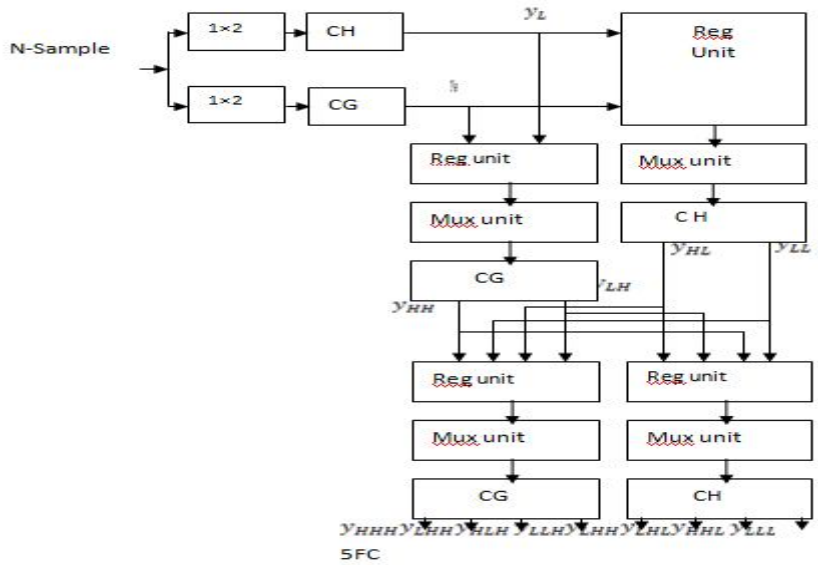

Figure: Complete 3-levels for DWPT. CG and CH are the CSD based high-pass and low-pass filters

4. COMPARISION

Comparison of theoretical result is up to third decomposition level architecture for DWPT.

Author	Multiplier	Adder / Sub	Shift register	Mux / De-mux	DAT
Zhang [1]	6	6	34	24	$4(T_m + 3T_a)$
Proposed (MB)	24	18	24	16	$T_m + 3T_a$
Proposed (CSDB)	-	51	24	16	$T_m + 3T_a$

We have implemented multiplier based (MB) architecture and canonic signed digit based (CSDB) architecture for DWPT by different approaches.

Author	Required time($nsec$)	Power (uW)	Area (um^2)	Area delay product (ADP) (um^2-sec)
Zhang [1]	87.64	396.1315	37249.3357	3264531.781
Proposed (MB)	36.80	385.1643	65477.7344	2409580.626
Proposed (CSDB)	26.80	223.16343	25477.3569	682793.165

5. Conclusion

In this dissertation, it is proposed that multiplier based (MB) architecture and canonic signed digit based (CSDB) architecture for Discrete Wavelet packet transforms (DWPT). We have used CSD number system to represent the filter coefficients of the wavelet filter with minimum number of ones. Consequently, the number of FAs of the design will be reduced by nearly 50% of these of the 2's complement design. Then we applied the CSD technique to further reduce the power and area. In this architecture the speed of the input sampling increased and used of the low and high pass filter. Low pass filter is the average between two sample and high pass filter is the difference between two samples. There is no on-chip memory and memory access during the computation, so that can achieve significant reduction in both die area and power dissipation.

In this dissertation, the proposed architecture is suitable for high speed on-line applications. With this architecture the speed of the wavelet packet transforms is increased, occupied areas of the circuit is reduced about 50% in the previous convolution based architecture and reduces the power about 15-25% in the previous convolution based architecture. It has 100% hardware utilization efficiency.

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