A Novel approach on design and development of high resolution (16 bit) analog input/output module with Hot Swap facility.

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Abstract

Computer Systems contributed to increased flexibility in design modification, reliability, ease of maintenance, reduced size complexity and cost compared to their hard-wired counter parts. Over the years several general purpose microprocessors based systems have been designed⁶ and developed for different real time applications. Initially to implement a certain feature or logic it would need the involvement of many ICs, which becomes obsolete and hence difficult in maintenance aspects. Progressively to reduce size and considering the maintenance, this logic is implemented in single IC and few devices that help us to implement logic like CPLDs and FPGAs¹. FPGA has enhanced productive quality, can be programmed to our requirements and has reduced hardware and hence is easy to maintain. Basically field signals are categorized into two types of signals namely Digital and Analog signals. There is need for development of a board which can process the analog signals and interface [⁴] with any Microprocessor which can run on a standard VME bus[⁵]. Thus to reduce the involvement of many ICs for implementation and for good maintenance, our proposed project emphasize on the development of an Analog board which can process 40 analog inputs, generate 8 analog outputs and a resolution of 16 bit. This board shall interface [⁴] with a power PC based processor[³]. MPC7447A[⁶] processors are ideal for leading edge computing, embedded network control[²] and signal processing applications.

IndexTerms—CPLDs, embedded network control, FPGAs, MPC7447A processor, 16 bit resolution, signal processing applications, VME bus.

1.Introduction

To design and develop standard hardware boards to meet the requirements these boards would be used extensively in all future reactor and non-reactor applications, they are to be designed based on present day technology and components in order to overcome obsolescence problem in the near future. Three major bus architectures for the design of these boards have been short listed. VME and an I/O bus were chosen for embedded system development and PCI bus for PC based system development owing to their popularity, availability of boards from multiple vendors and their prior experience with these architectures. A majority of embedded systems that have been developed so far in Reactor Control Division are highly I/O intensive and, in order to relieve CPU from I/O tasks, the I/O boards have been planned as intelligent I/O boards. To obtain higher density in terms of I/O and to minimize power consumption, it was decided to use SMD components and low voltage devices (3.3V). These I/O boards support hot-swap feature which is an essential requirement in power plants. This eliminates the need to put off a system for replacing a faulty I/O board. These boards support geographic addressing thus eliminating address related on-board jumpers. These boards have been designed with extensive self diagnostic features in order to detect faults on-line, thereby simplifying the system maintenance. Further, the sequencer is implemented on a FPGA using hardware description language so that any change in requirement can be easily incorporated. This board has been designed in such a way that it can be used either as Analog Input Board or as Analog Output Board. This board, when used as input board, accepts either 16 differential or 32 single ended inputs. Apart from this, it also accepts 4 test inputs for verifying the input circuit including the ADC. The inputs are digitized to 16 bit resolution. A quad DAC generates the test analog outputs that can be fed to the ADC for diagnostics purpose. In order to provide on-board isolation, the ADC and DAC data and control signals are passed over opto-coupler link. The control logic has been implemented on a FPGA. The control logic allows inputs to be read either on DEMAND mode or on AUTO mode. In AUTO mode, either all inputs or designated inputs are read continuously at a regular interval or once upon a trigger. The trigger source can be pacer driven, external or through software control. Control logic checks each digitized input against two set points (Low and High) and provide the complete status to the main CPU. When this board is used as an output board, it provides 8 voltage outputs. Provision to generate pre-determined (failsafe) output upon
detecting CPU failure is an added feature of this board. As part of self-diagnostics, these outputs are read back by the ADC for verification purpose.

1.2. Block diagram

2. Board Description

2.1. Features Of Board

The Analog input/output board is an improvised version of its preceding boards. It is a 6 layered user friendly board that incorporates a wide variety of possibilities for the present and the future. The salient features of this board can be stated as follows:

1) The speed of the board is 1 MSPS in the Warp mode and 800 KSPS normal mode. It uses a 16 bit A/D converter.
2) The board can accept 16 differential / 32 single ended field analog inputs.
3) It supports Auto scanning and Demand scanning. In auto scanning it goes on scanning specified number of channels for specified no of times once started. In demand scan it scans one channel on demand.
4) Again auto scan can run in auto sequence or random sequence. In auto sequence mode the scanning is started form a specified channel and goes on in ascending order for the number of channels to be scanned. In random sequence user can decide any random sequence for scanning.
5) The board produces 8 analog outputs.
6) It also incorporates 8 analog test inputs, which can be connected to external inputs or to read back the analog outputs.
7) Input/Output control logic is implemented in an FPGA.
8) The board can work as a slave board only.
9) This high performance module features high density I/O with a flexible topology and hot-swappable functionality.
10) A wide range of flexible signal conditioning types per channel are also offered. These include options such as RC filters on each input, voltage dividers on each input, 4-20mA current inputs, thermocouples (temp sensor for cold junction), RTD measurement, as well as bridge completion.
11) Additional features include software auto calibration (real-time) and on-board references for increased accuracy. Extended temperature (-40°C to +85°C) is available.
12) All models incorporate two 16-bit analog outputs, 16 lines of digital I/O that are integrated inside a small sized steel enclosure with an anti-skid bottom. A DIN rail mounting provision is available for installation in industrial environments.

The functional units of the Analog I/O board include:

- Connectors(P1&P2)
- RC Filters
- Multiplexers
- Jumpers
- ADC
- Isolators
- FPGA
- DAC
- Buffers.
3. Experimental analysis

3.1. Input Section
The input section of the Analog I/O board plays a vital role in the immaculate functioning of the board. It acts as a feeder from the field to the FPGA-which is the heart of the module. It comprises of connector, RC filters, Jumpers, ADCs (successive approximation type- AD7671).

3.1.1. Connector:
The connector P1 connects the inputs from the field to the network of RC filters. The connector P1 consists of three slots i.e., P1A, P1B and P1C. The positive connections are given to the P1A and the negative connections are given to P1C. The P1B slot has no connections. It is mainly for future scope to extend the number of inputs.

3.1.2. RC Filter:
The RC filter section consists of the main components that connect the input from the connectors to the multiplexers. It performs the important function of passing only the required signal to the many to one convertor which helps in preserving the overall gain of the signal.
The voltage across the capacitor is $V_C = I/C$. The voltage across the series combination is $V_{RC} = I (R^2 + (1/ωC)^2)^{1/2}$, so the gain is $g = 1/(1+ (ωRC)^2)^{1/2}$.

3.1.3. Multiplexer:
The multiplexers used for the Analog I/O board are AD408 and AD409. These are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG408 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1, and A2. The ADG409 switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When the device is disabled, all channels are switched off. The ADG408/ADG409 are designed on an enhanced LC2MOS process that provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.
The ADG408/ADG409 are improved replacements for the DG408/DG409 analog multiplexers.

3.1.4. Jumper:
A jumper is a short length of conductor used to close a break in, or bypass part of, a circuit. Jumpers are typically used to set up or adjust, such circuit boards as in computers. Jumper pins (points to be connected by the jumper) are arranged in groups called jumper blocks, each group having at least one pair of contact points. An appropriately sized conductive sleeve called a jumper, or more technically, a jumper is slipped over the pins to complete the circuit.
The jumpers used for the design of the Analog I/O board are shown above. The CON3 can drive up to four servo motors like those used in radio controlled airplanes and cars. The servo motors can be powered by 4.5V to 6V sources, while being controlled with TTL-level logic signals. The CON3 can be used in conjunction with Digilent system boards and embedded controller boards for robotics and distributed systems. The CON3 can be used with most servo motors including those that deliver anywhere from 50 to 300 ounce/inches of torque. Servo motor power can come from a system board (for low power applications) or from an external power source (for higher-power applications). A jumper setting determines the power source. Servo motors attached to the CON3 can be driven individually or in groups of two or more. Servo motors are used in a number of robotic applications, including steering, movement, and rotation. Servos are designed to move to a precise desired position and then stop. The CON3 has a power jumper that routes power to the servo motors through either the 6-pin header or a screw terminal (when using an alternate power source). When the power jumper is in the VCC position it routes power through the 6-pin header. When the power jumper is in the VE position it routes power through the screw terminal. When plugging a servo motor into the CON3’s servo connector, the white or yellow wire of the servo should connect to the signal portion of the connector, and the black wire should connect to the ground portion of the connector. The CON3 has a 6-pin header for easy connection to a Digilent system board. For example, some system boards like the Digilent Pegasus board have a 6-pin header that can connect to the CON3 with a 6-pin cable. To connect the CON3 to other Digilent system boards, a Digilent Modular Interface Board (MIB) and a 6-pin cable are needed. The MIB plugs into the system board, and the cable connects the MIB to the button module.

3.1.5. ADC:
The ADC used in the Analog I/O module is ADC7671. The AD7671 is a 16-bit, 1 MSPS, charge redistribution SAR, analog-to-digital converter that operates from a single 5 V power supply. It contains a high-speed 16-bit sampling ADC, a
resistor input scaler which allows various input ranges, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports. The AD7671 is hardware factory-calibrated and is comprehensively tested to ensure such ac parameters as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity. It features a very high sampling rate mode (Warp) and, for asynchronous conversion rate applications, a fast mode (Normal) and, for low power applications, a reduced power mode (Impulse) where the power is scaled with the throughput. It is fabricated using Analog Devices’ high-performance, 0.6 micron CMOS process and is available in a 48-lead LQFP with operation specified from –40°C to +85°C.

3.2 Control Section
The control section consists of FPGA. Field-Programmable Gate Arrays (FPGAs) are pre-fabricated silicon devices that can be electrically programmed to become almost any kind of digital circuit or system. They have many advantages over Application Specific Integrated Circuits (ASIC). ASICs are designed for specific application using CAD tools and fabricated at a foundry. Developing an ASIC takes very much time and is expensive. Furthermore, it is not possible to correct errors after fabrication. In contrast to ASICs, FPGAs are configured after fabrication and they also can be reconfigured. This is done with a hardware description language (HDL) which is compiled to a bit stream and downloaded to the FPGA. The disadvantages of FPGAs are that the same application needs more space (transistors) on chip and the application runs slower on a FPGA as modern as the ASIC counterpart. Due to the increase of transistor density FPGA were getting more powerful over the years. On the other hand the development of ASICs was getting slower and more expensive. Therefore FPGAs are increasingly applied to high performance embedded systems. Conceptually it can be considered as an array of Configurable Logic Blocks (CLBs) that can be connected together through a vast interconnection matrix to form complex digital circuits.

C. Interface Section
The VME & IO bus based Analog I/O boards includes:-
- BUS – FPGA Interface
- FPGA- Analog Input Interface
- FPGA- Analog Output Interface

Bus-FPGA Interface:-
Analog I/O Board has been designed for both VME and IO bus. VME bus interface is a slave board supporting A24, D16 addressing and data transfer mode. Five on-board dip Switches do address selection for board. IO bus is modified VME standard bus. It is asynchronous bus and uses same set of signals as of VME. Geographical addressing will be provided through jumpers to assign individual addresses for each board.

FPGA-Analog input interface:-
Xilinx XC3s400 FPGA is used to control & generate Chip Selects, SOC, read data and other control signals to ADC. ADC used is AD7671 from Analog devices. The AD7671 is a 16 bit, 1 MSPS, charge redistribution SAR, analog to digital converter that operates from a single 5 V supply. ADC uses an external 2.5 V voltage reference input. ADR421 is used for generating 2.5V reference. The ADC is specified to operate with six full-scale analog input ranges (refer the ADC data sheet for more details). Using on board dip switches one can do the various full-scale range selections. AD7671 features a very high sampling rate mode (Warp), for high accuracy application Normal mode and, for low power applications a reduced power mode (Impulse). The AD7671 needs a driver amplifier, which is AD829 from Analog Devices. The Multiplexer block consists of high performance analog multiplexer (mux) ADG408/ADG409 from Analog Devices.
Devices. ADG408 comprises of 8 single channels and the ADG409 comprises of 4 differential channels. Four Mux (1-4) are used to multiplex 16 differential and 32 single ended analog inputs. Mux 5 is used to handle the differential signals and Mux 6 serves to provide DAC channels feed back / Auxiliary input functionality in Analog Output section. The differential outputs of the ADG409 are taken into PGA 203, which is an instrumentation amplifier with digitally controlled gains of 1, 2, 4 and 8.

3.2 MUX-ADC interface:

3.3 FPGA-DAC interface

FPGA-Analog Output Interface:
DAC7744 is a 16 bit, quad voltage output digital to analog converter. It accepts 16 bit parallel input data. Xilinx FPGA is used to control and generate chip selects, DAC load, write, reset and other control signals to the DAC. Two DACs are used on the board to have 8 analog output channels. The DAC 7744 needs two precise voltage references VREFH and VREFL.

3.4 Output section

FPGA-Analog Output Interface:
DAC7744 is a 16 bit, quad voltage output digital to analog converter. It accepts 16 bit parallel input data. Xilinx FPGA is used to control and generate chip selects, DAC load, write, reset and other control signals to the DAC. Two DACs are used on the board to have 8 analog output channels. The DAC 7744 needs two precise voltage references VREFH and VREFL.

4. HOT SWAP
Hot Swap products from Analog Devices perform all the housekeeping functions necessary to hot swap plug-in boards. These parts also integrate with industry-leading converter and amplifier cores for power monitoring and control with patented circuitry delivering unmatched ± 3% monitoring accuracy. Hot swap controllers play a key role in keeping central office switching stations and server banks operating at peak efficiency. These devices safely and accurately monitor the power usage in atypical server rack system which enables oper boards to be safely inserted and removed from a live –48 V backplane. It features current, voltage, and power readback, and energy metering via an integrated 12-bit analog-to-digital converter (ADC), accessed using a PMBus interface. The part provides precise and robust current limiting and protection against both transient and nontransient short circuits and overvoltage and undervoltage conditions ators to remotely monitor each rack individually thus saving energy and minimizing system downtimes.
Analog Devices offers a variety of hot swap controllers including shunt regulated, low and high side FET drivers optimized for -48 V systems. There are also I2C interface hot swap controllers that allow for digital voltage and current data to be read from the device and power consumption for the rail to be calculated. Hot Swap evaluation software, design resources, tools, and online technical support can help shorten your design time. Designers can quickly select products based on key specifications with the Hot Swap parametric search tables. The ADM1075 is a full feature, negative voltage, hot swap controller with constant power foldback that allows boards to be safely inserted and removed from a live -48 V backplane. It features current, voltage, and power readback, and energy metering via an integrated 12-bit analog-to-digital converter (ADC), accessed using a PMBus interface. The part provides precise and robust current limiting and protection against both transient and nontransient short circuits and overvoltage and undervoltage conditions.

Fig 4.1: Hot swap functional diagram

5. Results and discussion
5.1 Programming and testing procedure:
Test Setup: All the inputs are simulated using the standard desktop PC and VME bus functionalities will be checked using a standard VME based I/O cards (CPU card) using a PC serial port and Ethernet port can write and read data from serial port. The board is tested by using Standard integrated software designed by DHRUVA in the PC.
To test the Analog Input output Board using FPGA, the FPGA has to be programmed. To program FPGA jumper J12 should be shorted and jumper J11 should be opened.
5.1.1 Programming of FPGA:
1. Connect Xilinx tool JTAG connector to pins available on the board.
2. Switch on the board
3. Open IMPACT software in the system then following dialog box will appear.
4. Click on cancel button, then following dialog box will appear.
5. Select Boundary Scan

6. Then right click to add device
7. And click initialize chain
8. Show the address of the test program to be programmed
9. Right click on device to perform operation
10. Click on the program
11. Then click ok

5.1.2 Software Testing:
To test AIO module tftp server and vme hyper terminal software are required.

5.2 Test result
5.2.1 Analog input output functionality test:
Using this test we can test Analog I/O card with hot swap. Analog inputs should be fed from precise variable voltage source. The +10V and -10V supply of the board is to be checked and adjust by measure voltage at TP36. Adjust R117 to get 10V. similarly measure voltage at TP55 and adjust R120 to make it -10V.

5.2.2 Testing of EHS boards:
1. Digital O/P on I/O bus
2. Protocol Translator Card
3. Generate BERR
4. Digital I/P on I/O bus
5. Analog i/o functionality
6. CPU Board Test
7. Relay Output Board
8. Test Hot swap
9. DATA Acquisition Board

Analog I/O functionality test is selected by Enter “5” then the following menu will appear:

Enter your choice: 5
Enter AIB address (16-bit): 0000

- Demand scan
- Auto scan
- DAC
- Check Reference
- AIO continuous RW
- Board Information

Check config Reg.

5.2.3 DEMAND SCAN:
Press ESC to go back to main menu….  
Enter your choice: 1
In Demand scan all the channels are scanned once on demand. The digital values are displayed in Hexadecimal as well as Voltage. The channel sequence can either be auto or random. That can be selected from following menu.

- Auto sequence
- Random sequence

Enter choice: 1  
When Auto sequence is selected scanning is done in increasing sequence starting from the first channel.

Auto sequence in demand scan
Press enter to continue scan
Channel delay (min: 5): 50
Here the delay between two channels to be given. Minimum value should be ‘5’ which corresponds to 50 micro volts.
Ch0: 7ff-> -0.000  ch1: 409-> -9.9684  
Ch2: 400-> -9.9687  ch3: 0 -> -10.0000  
Ch4: 0 -> -10.0000  ch5: 0 -> -10.0000  
Ch6: 0 -> -10.0000  ch7: 0 -> -10.0000  
Ch8: 0 -> -10.0000  ch9: 0 -> -10.0000  
Ch10: 0 -> -10.0000  ch11: 0 -> -10.0000  
Ch12: 0 -> -10.0000  ch13: 0 -> -10.0000  
Ch14: 0 -> -10.0000  ch15: 0 -> -10.0000  
Ch16: 0 -> -10.0000  ch17: 0 -> -10.0000  
Ch18: 0 -> -10.0000  ch19: 0 -> -10.0000  
Ch20: 0 -> -10.0000  ch21: 0 -> -10.0000  
Ch22: 0 -> -10.0000  ch23: 0 -> -10.0000  
Ch24: 0 -> -10.0000  ch25: 0 -> -10.0000  
Ch26: 0 -> -10.0000  ch27: 0 -> -10.0000  
Ch28: 0 -> -10.0000  ch29: 0 -> -10.0000  
ch30: 0 -> -10.0000  ch31: 0 -> -10.0000  

Readings should be within ± 2mV range of the actual input value.

AUTO SCAN:
When Auto scan is selected the scanning will continue automatically for specified number of times. Like Demand scan channel sequence can also be either automatic or randomly decided by the user. The sequence can be selected from the following menu.

Enter your choice: 2

- Auto sequence
- Random sequence

Enter choice : 1, then Auto sequence is chosen scanning will be done in increasing sequence starting from the first channel.
Auto sequence in Auto scan
Auto scan count in hex: 0000
Enter number of scans to be done. If 0 is entered scanning will continue infinitely.
Auto scan Interval in ms[min : 2ms]: 0000 Enter the interval between two scan in ms. Minimum value should be 2ms. It should be at least 40 times channel to channel delay.
Channel Delay (min: 5): 0005 Enter the delay between scan of two channels in 10s of microseconds.
Readings should be within ±2mV range of the actual input value

DAC:
Enter your choice: 3
Using this test we can check the function of DAC. The digital equivalent of the analog Outputs in Hex (7fff & ffff) are to be entered at the corresponding DAC0 through DAC7 and ensure the output voltage at the corresponding test jacks on the facial panel and check the values displayed after the read back.
Give DAC inputs
DAC0: 7fff (ffff)
DAC1:
DAC2:
DAC3:
DAC4:
DAC5:
DAC6:
DAC7:

DIGITAL VALUES AFTER CONVERSION
Data value DAC0: 0
Data value DAC1: 0
Data value DAC2: 0
Data value DAC3: 0
Data value DAC4: 0
Data value DAC5: 0
Data value DAC6: 0
Data value DAC7: 0

Analog Outputs should be measured at output. It should be within ±2mV range of the ideal value

CHECK REFERENCE
Enter your choice: 4
When read reference is selected ADC reference signal will be displayed.
Reference value: a000
Value should be within ±2mV range of the ideal value.

AIO CONTINUOUS RW
Enter your choice: 5
This is to test there is no mismatch in continuous write read.
If error is '0' then operation is OK.
ERR1: 0 ERR2: 0
ERR1: 0 ERR2: 0
ERR1: 0 ERR2: 0
ERR1: 0 ERR2: 0
ERR1: 0 ERR2: 0.

6. Summary:
This paper has presented a novel approach on design and development of high resolution (16 bit) analog input/output module with HOT SWAP facility. Earlier, Design, Development and Manufacturing of various complex control systems was based on Hard-Wired logics. As newer technologies became available computer based control and Information Systems are built around various popular Microprocessors like INTEL 8086, Motorola 6800 processors etc. The varieties of Input and Output boards have also been designed to support the microprocessor based control systems. The systems follow standard EURO bus/VME bus architecture based on the applications. There is need for development of a board which can process the analog signals and interface with any Microprocessor which can run on a standard VME bus. This paper emphasise on the development of an Analog board which can process 40 analog inputs, generate 8 analog outputs and a resolution of 16 bit. The board shall interface with a power PC based processor. MPC7447A processors are ideal for leading edge computing, embedded network control and signal processing applications, thus progressively reducing chip size and the number of Ics involved, improving the maintenance, improving product quality, software requirements can
be programmed which in turn reduces hardware. Hence, this paper reduces the real time problems and enhances the board increasing flexibility and is economical for usage, reducing the hardware components.

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