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A Novel Twenty Seven Level Asymmetrical Multilevel Inverter Using Cross Bridges

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Abstract

Multilevel inverters which are best known for their efficient performance in medium voltages and high power applications are best served in industrial and other purposes. In this paper, a multilevel inverter of twenty seven level is designed with a combination of cross bridge and a H-bridge which results in a stepped alternating voltage output with desired minimum total harmonic distortion, the output results are examined through MATLAB/ Simulink . Comparisons between various types of carrier waves along with PWM techniques.

Keywords: Multilevel inverter, Power Electronics, THD, Asymmetric, Cross bridge, H-bridge

1. INTRODUCTION

MULTILEVEL power conversion has been initiated and were being used since two decades . The general concept which is dealt in this topic is to utilize a higher number of active semiconductor switches to execute the power conversion in small voltage levels [1]-[10]. Nowadays, multilevel inverters are being found more attention in industries and academics as one of the adopted choices in electronic power conversion for high as well as medium power applications. They have successfully made their path into the industry and therefore it can be considered as a proven technology [11]-[12]. At present, we find them as standard and customized products that power a wide range of high and medium power applications. Some of their applications involve compressors, pumps, mills, fans, conveyors, crushers, turbine starters, marine propulsion, HVDC transmission and has also shown its importance in railway traction and in many more areas [1].

As we know, a conventional inverter is an electrical device which converts dc power into ac power. This inverter is generally used for emergency backup power in households and also for many other electrical devices in various industries. The main reason to adopt a multilevel inverter rather than a conventional inverter is that it has only two output voltage levels which are depicted as a square wave and also due to its higher total harmonic distortion. If the input is provided with voltage of 100V, then the output will be of two levels which are +100V and -100V. This results in a square wave output in which the distortion to an actual ac output sine wave will be very high. To overcome this disadvantage, the concept of multilevel inverter is discovered and implemented. A multi level inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower level DC voltages as input. Also, many applications in industries require high power and medium power for their operation. Using a high power source for all the industrial loads may be beneficial for high power loads while it may cause irreparable damage to the other loads. To overcome these type of situations, multilevel inverters came into light.

A multilevel inverter (MLI) is a linkage structure of multiple dc levels as input and power semiconductor devices to incorporate a staircase waveform with reduced voltage stresses when compared to its overall operating voltage [11]-[13]. An MLI waveform also has a better harmonic profile as compared to a two – level conventional inverter. Other advantages of MLIs are reduced dv/ dt stress on the load, allows operation at higher voltages as the semiconductors are wired in series-type connection, reduction in electromagnetic compatibility and also the possibility of fault-tolerant operation. The efficiency of a multilevel inverter increases only when the levels increase. However, it coincidentally leads to a large number of power semiconductor devices along with gate driver circuits. This increases the complexity as well as the cost of the system and tends to reduce the system's reliability and efficiency. For a high resolution

waveform, there is a necessity of reduction in the number of switches and gating circuits. Research is being carried out to reduce the number of power switches while increasing the levels and also to employ MLIs for low-power applications.

The topologies which have been widely studied and are commercially available for multilevel voltage output are neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC) converters. The approaches carried out by researchers to modify and enhance the performance of an MLI can be classified into three categories: topological changes, use of asymmetric sources, and combination of topological changes and asymmetric source configurations.

In this paper, a new topology is proposed in which asymmetric dc sources are linked to each other through cross-bridge switches. This approach significantly lessens the number of power switches and the total harmonic distortion by increasing the number of levels. This topology also includes a H bridge which is connected to the load. The proposed topology is a combination of cross bridge and H bridge configurations. Thus, the topology can be used as a utility interface for any kind of dc sources available. This paper is organized as follows. Section 2 and 3 presents the generalized structure of the proposed topology including its switching scheme along with the switching pulses of each switch. Section 4 describes about the operation and the principle of the topology is also described in this section. . In Section 5, the mathematical modeling for the proposed topology is described. The simulation results are presented in Section 7. Conclusions are summarized in Section 8 along with references.

2. PROPOSED TOPOLOGY

The proposed inverter is advantageous compared to a general cascaded H- bridge MLI because the arrangement of power switches is a combination of both cross bridge and H-bridge. This type of arrangement provides us with increased number of levels with same or less number of power switches that has been used to construct a standard H-bridge multilevel inverter. Thus, on decreasing the number of power switches, the power losses associated with the semiconductor devices also decreases which ultimately helps in enhancing the power quality of an MLI waveform. The general structure of the proposed topology is shown in Figure 1.

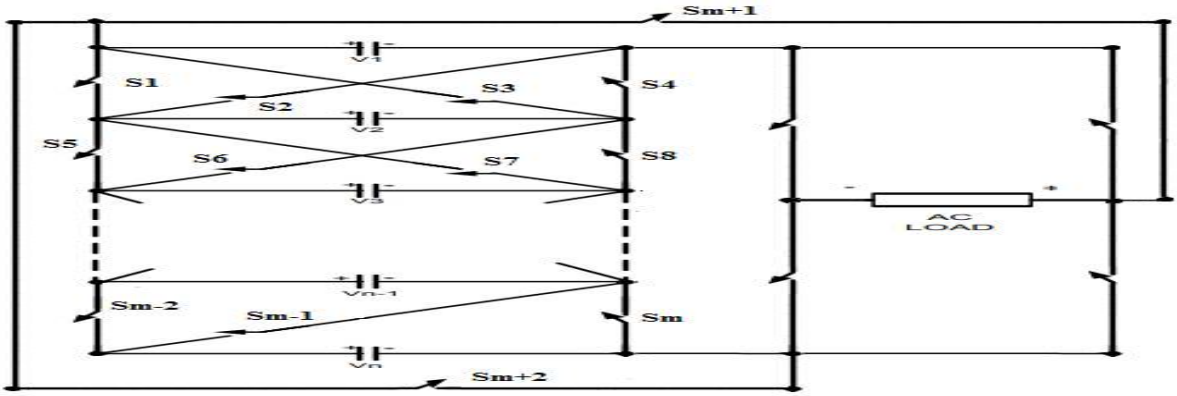

Figure 1 Proposed multilevel topology with 'n' sources

The proposed multilevel inverter configuration is designed with 13 switches and 3 asymmetric DC sources. This circuit consists of one H-bridge with four main switches and seven auxiliary cross bridged switches along with two switches on either side of the H-bridge. In this inverter, IGBT is used as a semiconductor device as it holds the combine features of both MOSFET and BJT with lower switching losses. Each switch requires its own gate driver circuit. The arrangement of switches and DC sources is made in such a way that it is possible to obtain all the practicable combinations of DC voltages (both additive and subtractive) in the output. For H-bridge, switch pair S9 and S10 works for positive half cycle and switch pair S8 and S11 works for negative half cycle with three ternary DC voltage sources i.e., Vdc, 3Vdc and 9Vdc. The proposed structure for twenty seven level inverter is shown in Figure 2.

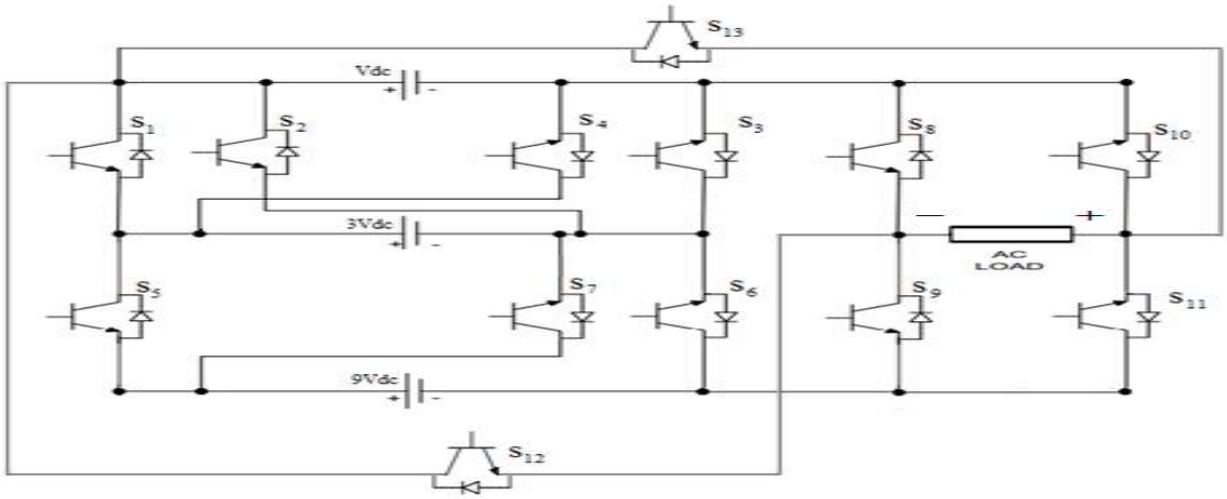

Figure 2 Proposed structure for twenty seven level MLI

3. SWITCHING SCHEME AND PULSES

Pulse-width modulation (PWM) is the most productive means to attain a constant voltage battery charging by switching the system controller's power devices. Pulse Width Modulation refers to a procedure of carrying information on a train of pulses, the information is encoded in the width of the each pulse. This technique helps in maintaining a constant voltage.

For an n level inverter, (n-1) carriers with same frequency fc and same peak to peak amplitude Ac are used. The reference waveform has amplitude Am and frequency fm and it is centered at zero level. The reference wave is continuously compared with each of the carrier signals. If the amplitude of the reference wave is greater than that of a carrier signal, then the active devices corresponding to that carrier is switched ON otherwise, the devices switch OFF.

In this topology, phase opposition disposition strategy is used in which all the carriers have same frequency and amplitude, but all the carriers above the zero reference are same in phase and the carriers below the zero reference are 180 degree phase shifted with respect to each other. For this topology, a single waveform and 26 triangular carrier waveforms are used. Carrier and reference arrangements for this twenty seven MLI are shown in Figure 3.

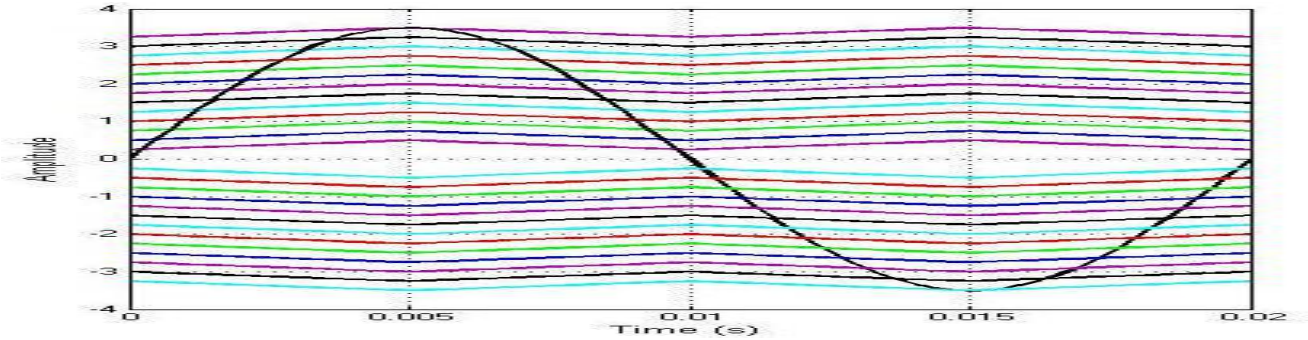

Figure 3 Portrayal of the phase opposition disposition PWM technique used

We can define other parameters such as modulation index and frequency ratio on using this modulation technique. .
The modulation index is defined as

$ma = (2A_m) / ((n-1)A_c)$ .. (1)

The frequency ratio is defined as

$m_f = f_c / f_m$ .. (2)

where, f_c = carrier frequency
f_m= Frequency of the reference wave
A_c = Amplitude of the carrier wave
A_m = Amplitude of the reference wave

Here, f_c = 100 Hz f_m = 50 Hz

$A_c = 0.25$ $A_m = 3.5$
Therefore, from (1) and (2)
Modulation index (m_a) = 1.08
Frequency ratio (m_f) = 2

In order to synthesize the stepped output waveform from input DC source, the power switches must be triggered ON and OFF in different time periods for various voltage levels. The gating circuit is provided to each semiconductor device to get triggered and to produce the output waveform. However, some set of switches are triggered ON for positive half cycle and another set of switches are triggered ON for negative half cycle. Hence, the switching pulse for each power switch will be non-identical. The gate triggering circuit is simulated with input DC voltage sources of 1V each. Figure 4. shows the switching pulses of the switches involved in the first cross bridge.

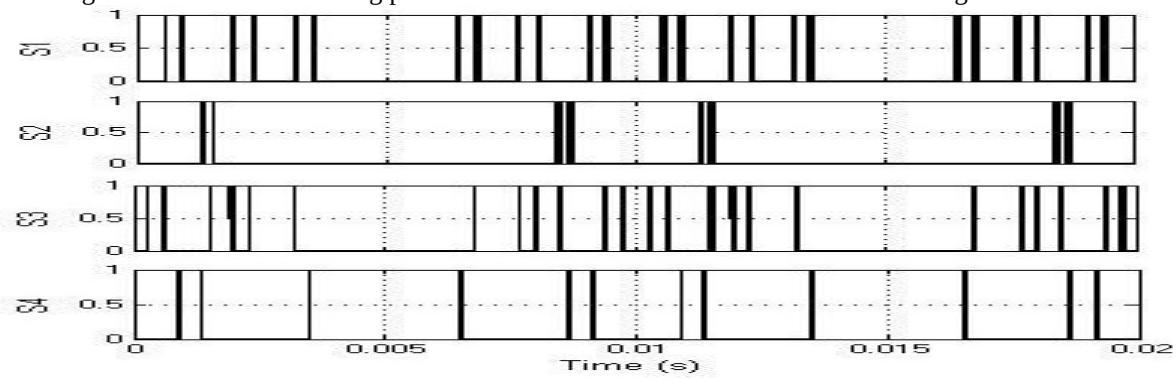

Figure 4 Switching pulses of cross bridge switches

The cross bridge in this topology involves power switches S1, S2, S3 and S4. The H-bridge in this configuration involves power switches S8, S9,S10 and S11. The switching pulses of the switches included in the H-bridge are shown in Figure 5.

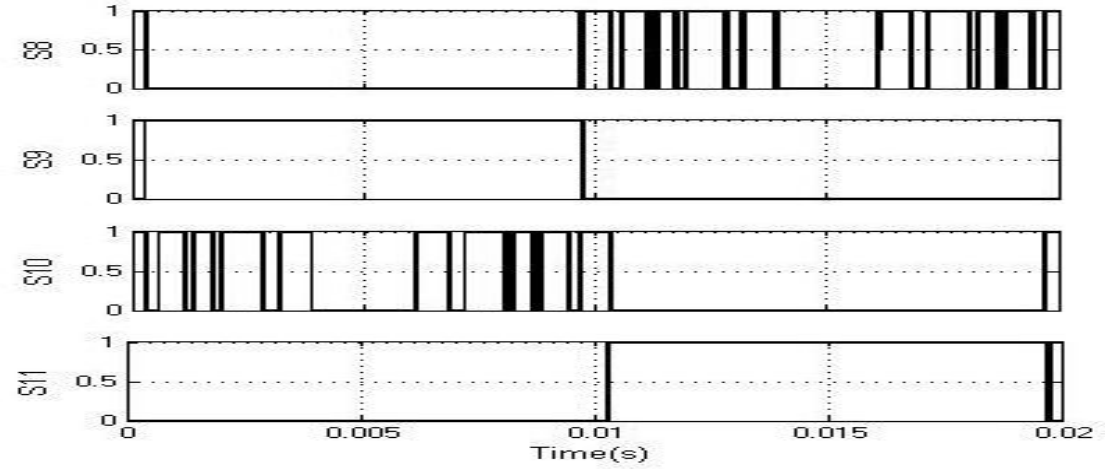

Figure 5 Switching pulses of H-bridge switches

4. OPERATION

switches and DC sources. By decreasing the number of components, we will be able to reduce the switching losses and also the complexity of the circuit. In the proposed topology, we have used 4 asymmetrical DC voltage sources of cubic form which are 1V, 3V, 9V, 27V along with 17 number of igbt switches.
The proposed topology can be formulated into a general form which can be used to determine particular number of levels by using particular number of switches or sources.

The number of levels obtained using the proposed topology with 'n' number of DC voltage sources can be determined by,

..(11)

where,
N = Number of voltage levels obtained

n = Number of DC voltage sources
The number of switches needed to design an N level MLI using the proposed topology with 'n' number of DC voltage sources cam be determined by,
S = 4n+1 ..(12)
where,
S = Number of switches needed
n = Number of DC voltage sources

5. SIMULATION RESULTS AND COMPARISONS

Multi-carrier phase opposition PWM control strategy has been used to simulate the proposed configuration for single phase operation of the load with three DC input voltages. The DC voltages V1, V2, V3 are taken to be 1V, 3V and 9V respectively. The voltage levels are from the load is taken to be an R load with the value of the resistance to be 100Ω . With these three voltage sources, the possible number of voltage combinations(both positive and negative) is twenty seven. The amplitude and the frequency of the reference wave is 3.5 and 50 Hz.
The amplitude and frequency of each carrier wave is 0.25 and 100 Hz. The modulation scheme consists of one reference wave and twenty six triangular carrier waves. The semiconductor device used in this circuit is IGBT and each switch is triggered with 1V DC Voltage source. Each switch has a resistance of 0.001 Ω and a snubber capacitance as infinity along with snubber resistance of 100KΩ. The staircase output waveform of this inverter is shown in Figure 6

6. MATHEMATICAL MODELLING

The key point in designing a Multi-level inverter is to obtain maximum number of levels by using less number of switches and DC sources. By decreasing the number of components, we will be able to reduce the switching losses and also the complexity of the circuit. In the proposed topology, we have used 4 asymmetrical DC voltage sources of cubic form which are 1V, 3V, 9V, 27V along with 17 number of igbt switches.
The proposed topology can be formulated into a general form which can be used to determine particular number of levels by using particular number of switches or sources.

The number of levels obtained using the proposed topology with 'n' number of DC voltage sources can be determined by,
$N = 3^n$ ..(11)
where,
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n = Number of DC voltage sources
The number of switches needed to design an N level MLI using the proposed topology with 'n' number of DC voltage sources cam be determined by,
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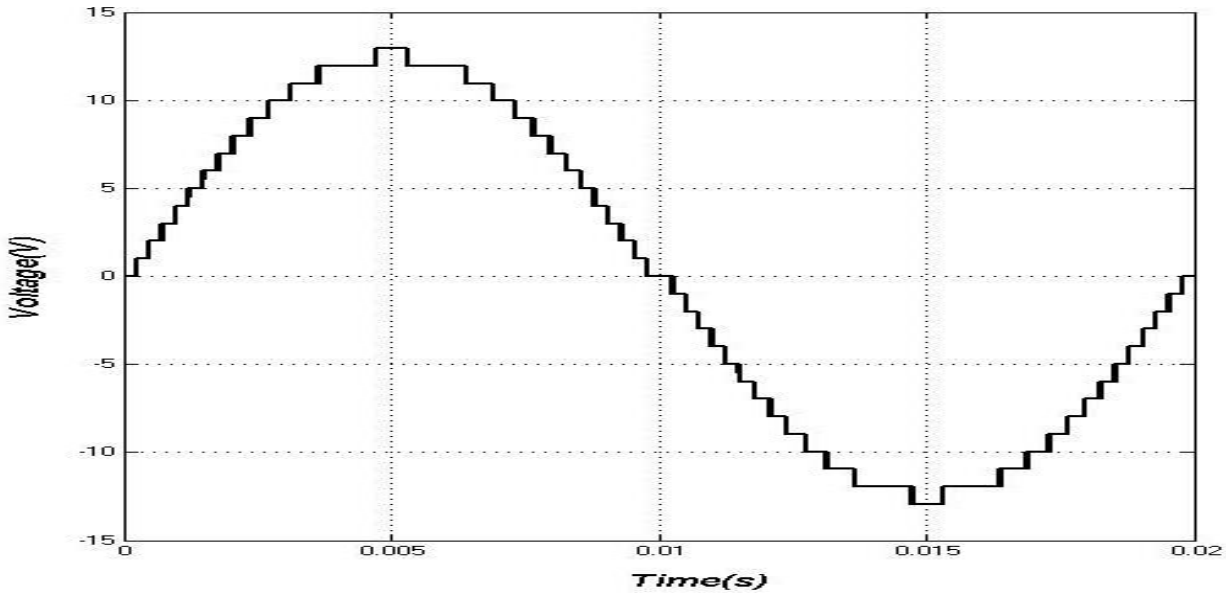

Figure 6 Output waveform of proposed topology

The Fast Fourier transformation (FFT) analysis of the output is represented as a bar graph which is shown in Figure 7.

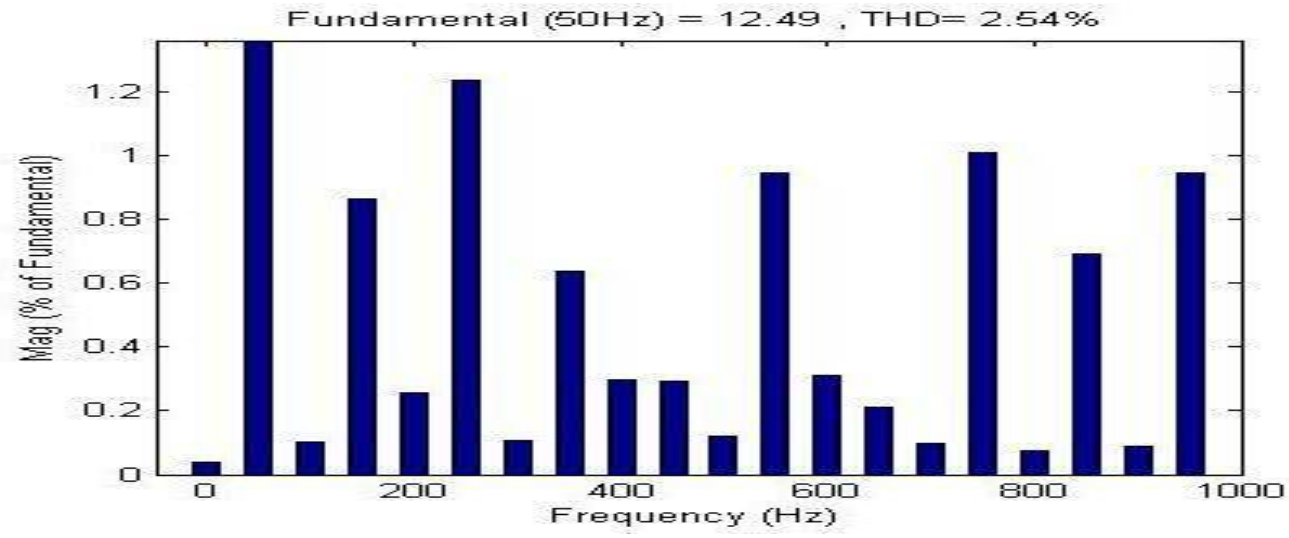

Figure 7 Bar graph of FFT analysis

The fundamental frequency, THD percentage and the percentage of all the harmonics present in the output waveform is shown as a list in Figure 8.

```
DC component          = 0.004955
Fundamental           = 12.49 peak (8.833 rms)
THD                   = 2.54%

      0 Hz    (DC):          0.04%      90.0°
     50 Hz    (Fnd):       100.00%      -0.0°
    100 Hz    (h2):          0.10%     -30.0°
    150 Hz    (h3):          0.87%     175.0°
    200 Hz    (h4):          0.25%      -2.6°
    250 Hz    (h5):          1.24%     183.1°
    300 Hz    (h6):          0.11%     140.4°
    350 Hz    (h7):          0.64%     179.1°
    400 Hz    (h8):          0.30%     194.8°
    450 Hz    (h9):          0.29%     169.7°
    500 Hz   (h10):          0.12%     164.7°
    550 Hz   (h11):          0.95%     184.8°
    600 Hz   (h12):          0.31%       6.3°
    650 Hz   (h13):          0.21%      13.8°
    700 Hz   (h14):          0.10%     233.0°
    750 Hz   (h15):          1.01%     179.3°
    800 Hz   (h16):          0.08%     119.6°
    850 Hz   (h17):          0.69%      -5.6°
    900 Hz   (h18):          0.09%     186.0°
    950 Hz   (h19):          0.94%     175.4°
```

8. COMPARISON OF THD BETWEEN TYPES OF MODULATION TECHINIQUES AND TYPES OF CARRIER WAVES

The total harmonic distortion as well as the harmonic components varies as we change the type of modulation technique or the type of carrier wave used. The comparison of THD between different types of carrier waves for each Pulse width modulation technique is presented below.

8.1 Phase disposition PWM Strategy

In this method, all the carrier waves above and below the zero reference line (both positive and negative carrier waves) are in phase. The graphical representation of this strategy using a triangular carrier wave is shown in Figure. 9. On using this technique, the variation of THD upon using different types of carrier wave i.e. triangular wave, trapezoidal wave, saw tooth and reverse saw tooth wave are presented in the bar graph shown in Figure 10.

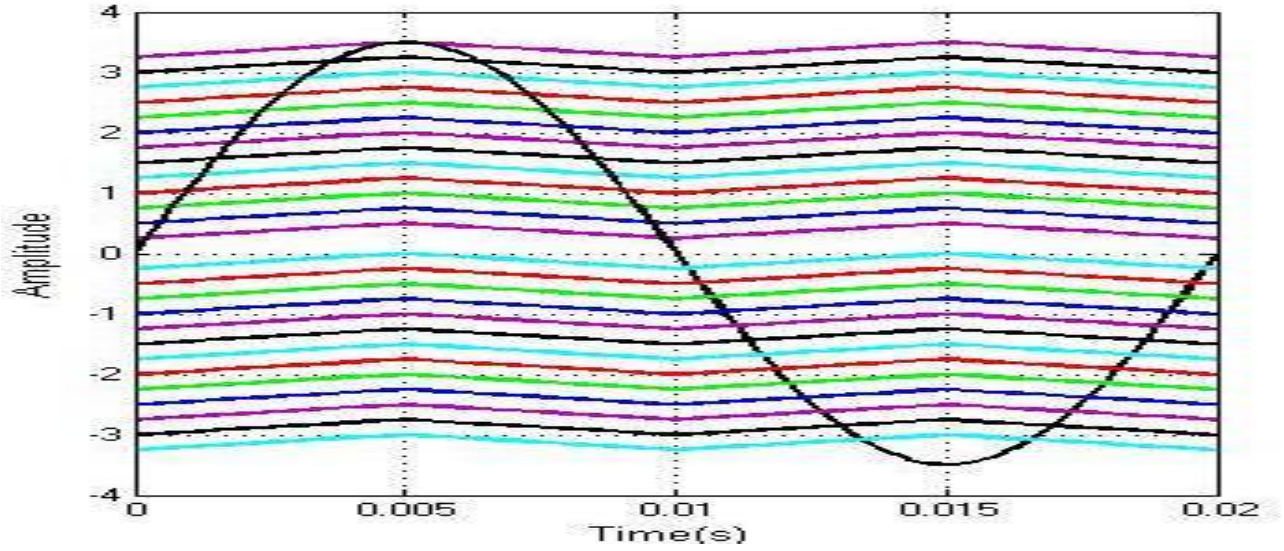

Figure 9 PDPWM technique with triangular wave

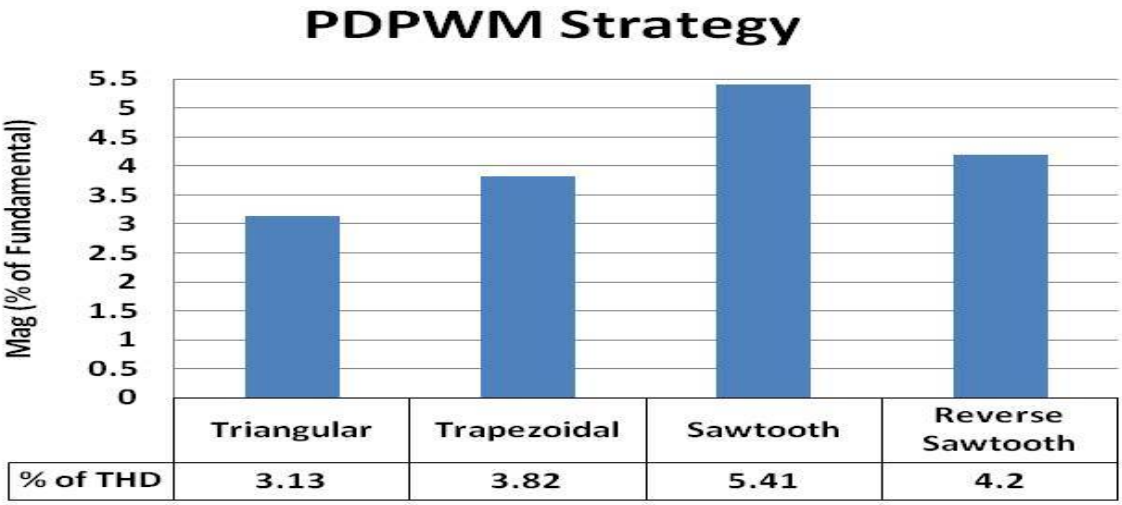

Figure 10 Comparison of THD for PDPWM technique with different carrier waves

8.2 Phase Opposition Disposition PWM Strategy

In this method, all the carrier waves have same frequency and amplitude, but the negative carriers are 180 degree out of phase with positive carriers. The graphical representation of this strategy is shown in Figure 11. On using this technique, the variation of THD upon using different types of carrier wave i.e. triangular wave, trapezoidal wave, saw tooth and reverse saw tooth wave are presented in the bar graph shown in Figure 12.

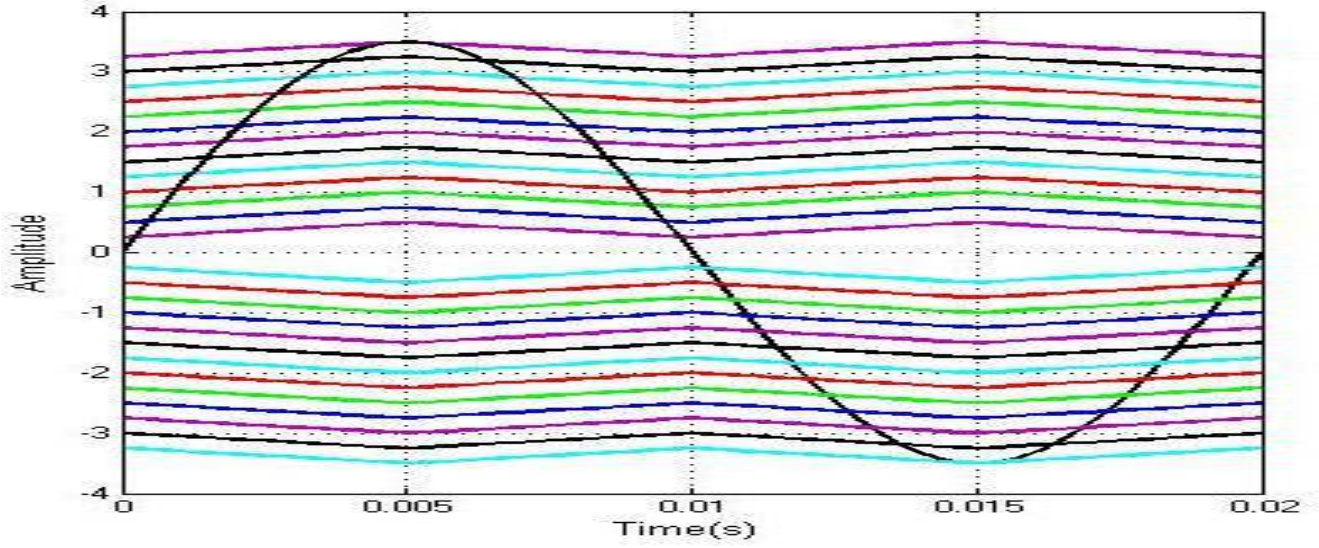

Figure 11 PODPWM technique with triangular wave

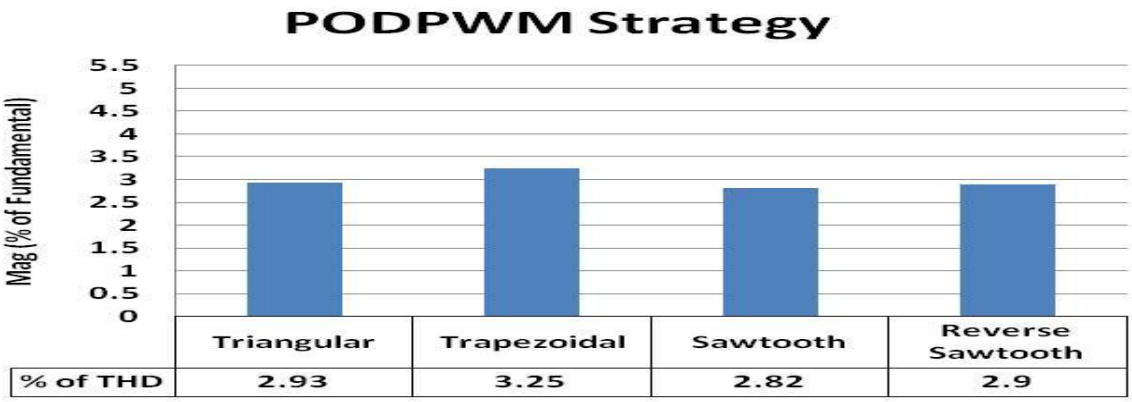

Figure 12 Comparison of THD for PODPWM technique with different carrier waves

8.3 Carrier Overlapping PWM Strategy

In this overlapping method, carriers with the same frequency and same peak to peak amplitude are disposed such that they occupy overlap each other, the overlapping vertical distance between each carrier is Ac/2. The reference waveform is centered in the middle of the carrier signals. The modulation index ma is defined as

$$ma = 2A_m/(n-3)A_c \quad ..(14)$$

The amplitude of the carrier wave (Ac) is taken to be 1.5 and the amplitude of the reference wave (Am) is 13.5. The frequency of the carrier wave is 500 Hz and that of the reference wave is 50 Hz. Thus the modulation index ma is 0.75. The graphical representation of this strategy is shown in Figure 13. On using this technique, the variation of THD upon using different types of carrier wave i.e. triangular wave, trapezoidal wave, saw tooth and reverse saw tooth wave are presented in the bar graph shown in Figure 14.

We must also note that the frequency is 100 Hz for the PDPWM and PODPWM strategies and the magnitude of the amplitude used for all the carrier waves in these techniques is 3.5.

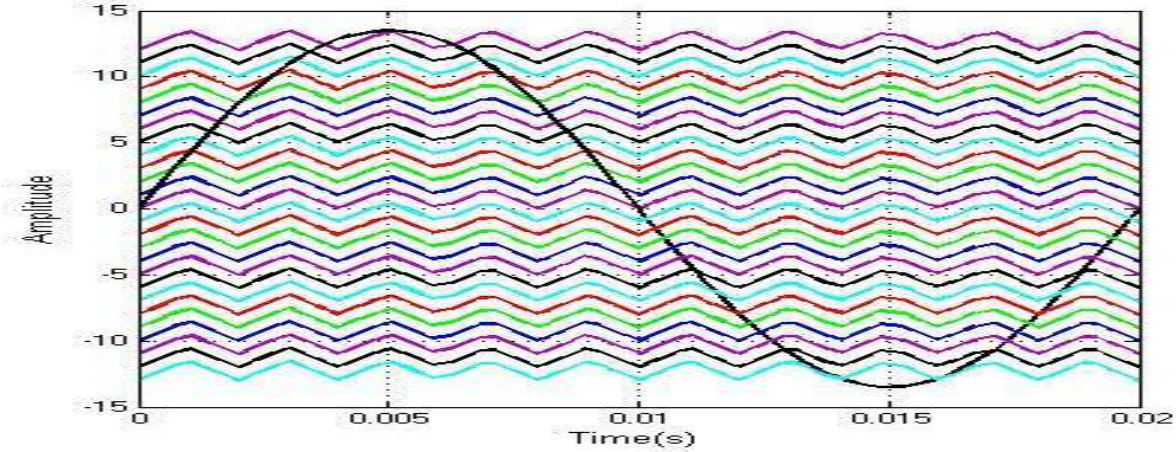

Figure 13 COPWM technique with triangular wave

Figure 14 Comparison of THD for COPWM technique with different carrier waves

6.CONCLUSION

This paper provides a design that is reliable and efficient as it gives more number of levels using least number of components possible. The proposed twenty seven level topology of combined cross bridges and H-bridge results in multiple number of paths which outcomes more number of levels, thus resulting lesser THD. From the FFT analysis, we can observe that total harmonic distortion of a twenty seven level multilevel inverter is 2.54% which is the inverter to give an effective lossless output ac voltage that is liable for many industrial applications.

The proposed topology can be effectively employed for applications such as conversion and control of electric power, static VAR compensation, motor drives, uninterruptable power supply (UPS), compressors, fans etc.

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