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# An Area Efficient secure solution Low Power High Speed from a Pulse Triggered Flip Flop Using Pass Transistor

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## ABSTRACT

***The performance of flip-flop is a very important part to see the potency of the total synchronous circuit. This paper presents associate economical specific periodical static single edge triggered flip flop with associate improved performance and overcomes the drawbacks of the implicit sort periodical flip flops. The projected flip flop has a structure of specific pulse-triggered with a changed true single part clock latch supported signal feed through theme. Flip-Flop (FF) is essentially used as a memory parts in Digital circuits like Microprocessors. within the gift situation, power consumption may be a major challenge in Digital style. FF is split into 2 stages, one stage is that the clock system and also the different may be a latch that that stores information during this paper, a completely unique low-power pulse-triggered FF {is styleed|is meant|is intended} by using 2 new design measures. the primary one with success reduces the quantity of transistors stacked on the discharging path by incorporating a PTL-based AND logic. The other supports conditional sweetening to the peak and breadth of the discharging pulse so the dimensions of the transistors within the pulse generation circuit may be unbroken minimum. Simulation results indicate that the projected style achieves low power and high speed with less space compared with standard flip flops.***