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Parameter analysis of ECRL & 2N2N-2P Energy Recovery Comparators

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Abstract

This paper presents a comparison study, modeling of low power comparator design based on adiabatic energy recovery logic. We have presented 2N-2N2P and ECRL based comparator designs. We have computed the power dissipation, delay, power delay product and energy saving factors of various adiabatic comparator structures. Adiabatic logic based circuit carry out less power consumption by constraining current flowing through devices with less voltage drop and by reusing the energy stored at output node instead of discharging it to ground. The designs are simulated using Cadence Virtuoso EDA Tool.

Keywords: Adiabatic, Comparator, CMOS, EDA, PASCL, PDP, ESF

1. INTRODUCTION

Low energy operation is vital in many portable and battery operated systems. Introduction of adiabatic logic, as an approach to minimize energy consumption of digital logic, has really taken off recently in the works of Athas,Koller and Svensson , Younis and Knight , Hinmanand Schlecht. The adiabatic logic circuits utilize power supplies to recycle the energy used to charge node capacitances in the circuit. Although many interesting approaches have been presented, several weaknesses of these circuits can be identified. The implementation is complex the logic gates are not well suited for CMOS technology multiple power-clock problems.

Minimizing the power dissipation is a rising problems at all levels. Such as circuits, logic, architecture, device technology and system levels. Out of this, one of the approaches is adiabatic logic [2]. Adiabatic logic is a new novel approach that has been invented for ultra low power digital circuits and systems. One of the advantages of adiabatic logic circuits is that while using adiabatic logic circuit, it will decrease overall power consumption as well as switching power of the system. Comparator is a combinational logic circuit that compares two inputs binary and gives outputs to indicate which one has greater magnitude. It is useful in control applications where a binary number representing the physical variable being controlled is compared with a reference value. Apart from operational amplifiers or OP-AMPs, comparators are most probably second most widely used electronic components in electronics industries. thi Comparators are referred to as 1-bit analog-to-digital converter which is widely used in ADC circuitry. The speed of comparator is very critical in digital systems which is limited by the decision making time of the comparator [3].

2. ADIABATIC LOGIC

Adiabatic logic is also known as energy recovery logic. An adiabatic logic is one that does not release energy when heat increase across the boundary of the device during its operation or working phase. The term adiabatic is derived from thermo dynamic process. Adiabatic logic has several different logic styles which are used to reduce the power consumption of the circuit. Adiabatic technology is basically used to reduce the energy dissipation during the switching process and further reuse some of the energy by recycling it from the load capacitance[1]-[3]. For recycling, the adiabatic circuits use the constant current source power supply and for reduce dissipation it uses the trapezoidal or sinusoidal power supply voltage Energy recovery principle can be best understood by fig 1.

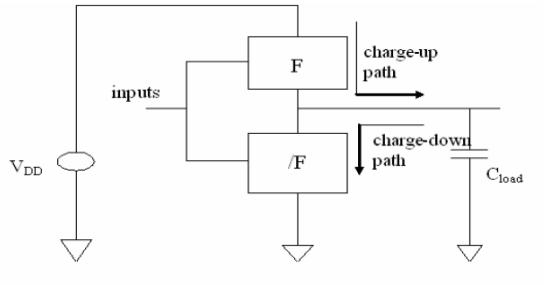

Figure1: adiabatic principle

Adiabatic logic families are generally categorized into two major groups as fully adiabatic logic and partially adiabatic logic. Adiabatic logic circuits can also be classified as transistor based adiabatic circuits and diode based adiabatic circuits. In fully adiabatic logic all the dissipated power is recycled and in partially adiabatic logic some of the power is recycled and some of the power is lost as heat. Some of the fully adiabatic logic families are Two Phase Adiabatic Static Clocked Logic (2PASCL) Pass transistor Adiabatic Logic (PAL). Some of the partially adiabatic logic families are Efficient Charge Recovery Logic (ECRL), 2N-2N2P Adiabatic Logic and Positive Feedback Adiabatic Logic (PFAL). In this paper we have presented two partially adiabatic logics namely 2N2N-2P and ECRL logic.

3. EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

Each adiabatic system consists of two main parts, the digital core design made up of adiabatic gates and the generator of the power-clock signals. Efficient Charge Recovery Logic uses cross-coupled PMOS transistors. It has the structure similar to cascode voltage switch logic with a differential signalling. As the circuit uses differential logic, so each gate computes both a logic function and its complement, and each gate requires complimentary inputs [4] [10]. The ECRL consists of two cross-coupled transistors M1 and M2 and two NMOS transistors which are shown in Fig.1. An AC power supply known as power clock in case of adiabatic logic (PC) is used for ECRL gate to recover and reuse the supplied energy. Both out and complement out are generated to the power clock generator which drives a constant load capacitance independent of the input signal [2].Full output or complete output swings is obtained because of the cross-coupled PMOS transistors in both pre-charge and recover phases. Cross-coupled P type MOS transistors in both pre-charge and recover phases has been used to obtain the full output swings. However due to the threshold voltage (V_{th}) of the P type MOS transistors, the circuits recover from the non-adiabatic loss in the pre-charge and recover phases.

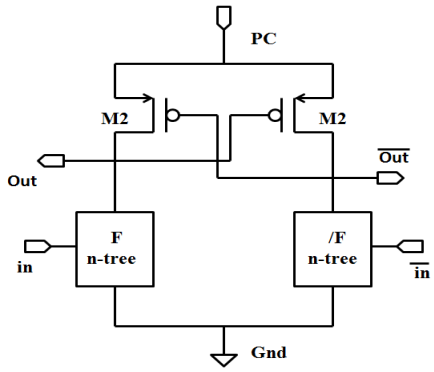

Figure2: ECRL inverter

4. 2N2N-2P Energy Recovery Logic

2N2N-2P adiabatic family belongs to the partially adiabatic logic family, derived from ECRL in order to minimize the coupling effect. Figure 2 shows the schematic of 2N-2N2P family. Its main advantage over ECRL is the cross coupling of NMOSFET switches which leads to non floating outputs for major part of the recovery phase. A variant of the ECRL logic family is 2N2N-2P family with the only difference that it has a pair of cross-coupled NMOS transistors in

addition to the cross coupled PMOS transistors. 2N2N2P family is very similar to a standard CMOS based SRAM cell as it has cross -coupled full inverters.This adiabatic logic family is obtained from Efficient Charge Recovery Logic (ECRL) in order to achieve state stability.

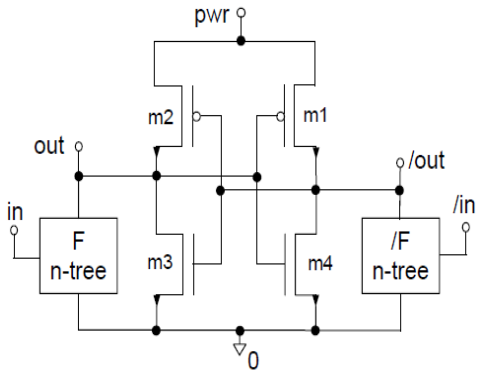

Figure3: 2N2N-2P energy recovery logic inverter

5. ECRL COMPARATOR

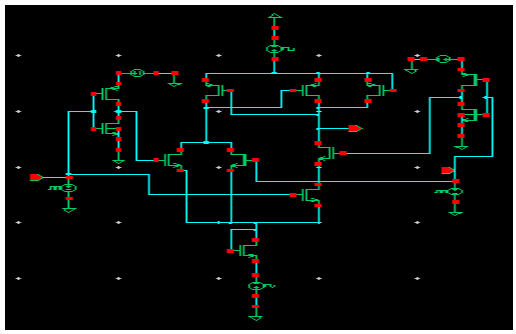

Figure4: ECRL comparator

The fig.4 gives the schematic diagram for combination of ECRL and 2PASCL based comparator. 2PASCL uses two split level complementary sinusoidal signals which operate in different modes like normal and recovery phase. It also has two diodes in its structure while comparing to ECRL. The core part is designed on the basis of ECRL which rapidly generate decision making signals. The designed comparator circuit has two input nodes, where the signals to be compared are given as input. These two inputs are designated as a and b. Depending on the input signals, the circuit has two output states low or high. If signal a is greater than signal b, one output node will charge to V_{dd}, and that node is designated as agb and another output node is alb. This decision is rapidly obtained by a transmission gate which separate power supply and functional block. The circuit consists of two phases of operation that is evaluation phase and recovery phase. During evaluation phase, normal comparison operation will take place only when power supply voltage swings up from 0 to V_{dd}. The recovery phase occurs when the power supply voltage swings down from V_{dd}. In this operation, the combination of ECRL and 2PASCL based comparator recover 50% of power discharged to ground.

6. 2N2N-2P COMPARATOR

The schematic diagram for combination of 2N2N-2P and 2PASCL based comparator is demonstrated in fig.5. The core part is designed on the basis of 2N-2N2P adiabatic logic in order to achieve state retention at the output node. The designed circuit has two input node where two signals to be compared is given. These two inputs are designated as *a* and *b*. Depending on the input signals, the circuit has two output states. If signal *a* is greater than signal *b*, one output node will charge to *Vdd* that node is designated to *agb* and another output node is *alb*. This decision is rapidly obtained by a transmission gate which separate power supply and functional block.

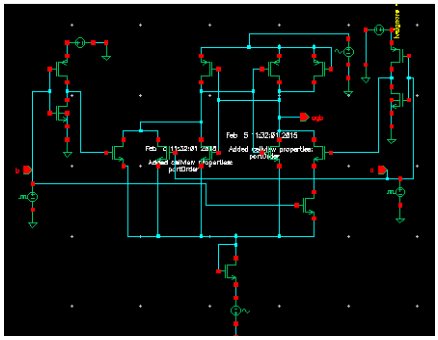

Figure:5 2N2N-2P comparator

7. SIMULATION RESULTS

We have simulated the comparator circuit using cadence EDA design tool. Power dissipation and propagation delays of both ECRL and 2N2N-2P comparators are measured. The power- delay products of both the comparators are also obtained. The observation frequency is 50MHz.

Table 1: Power dissipation of various comparator circuits

Circuit	**Power Dissipation**
ECRL	2.54nw
2N2N-2P	0.16nw
CMOS	12.35nw

Table 2: Delay calculation of various comparator circuits

Circuit	**Delay**
ECRL	6.23ns
2N2N-2P	0.22ns
CMOS	11.29ns

Table 3: PDP calculation of various comparator circuits

Circuit	**Power Dissipation**
ECRL	15.83
2N2N-2P	0.63

CMOS	139.49

Table 4: Energy saving factor (ESF) calculation of various comparator circuits

Circuit	**Power Dissipation**
ECRL	0.20
2N2N-2P	0.01

Here, in this work, sinusoidal power clock offers the effective use of power by providing the path to recycle or reuse energy at output node instead of discharged to the ground or dissipated as as heat and lost. This offers the great advantage in the reduction of the total power dissipation and also have green effects to the environment. We have presented different adiabatic logic based comparators which yield maximum power reduction compared to the previously available CMOS comparator. The presented design is simulated using Cadence Virtuoso Environment. The simulation results clearly show that the current design has much less power compared to the conventional CMOS comparators. The difference in energy saving factor also shown in this paper. We have also shown the main objective of our work which is comparison of two types of partially adiabatic or energy recovery comparators. Our results show nearly 80% saving of power for 2N2N-2P comparators. These low power comparators can be used in portable applications and other high speed ASICs.

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