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Super Conducting Magnetic Energy Storage DVR based on Diode Clamped Modular Multilevel Converters

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Abstract
The superconducting magnetic energy storage system (SMES) has been emulated by a high-current inductor to investigate a system employing both SMES and battery energy storage system (BESS). A series-connected three phase voltage source inverter used to regulate ac voltage, and two bidirectional dc/dc converters used to control energy storage system charge and discharge. "DC bus level signaling" and "voltage droop control" have been used to automatically control power from the magnetic energy storage system during short-duration, high-power voltage sags, while the battery is used to provide power during longer term, low-power under voltages. The SMES-BESS hybrid dynamic voltage restorer (DVR) can support both short-term high-power voltage sags and long- term under voltages with significantly reduced superconducting material cost compared with an SMES based system. The DVR is a fast and efficient solution to voltage sag problems. Here we use a new configuration of DVR which is based on the parallel diode- clamped modular multilevel converter (DCM2C). Where the capacitor voltages distributed in the sub-modules can be balanced automatically without any balancing control algorithms.

Keywords— Super Conducting Magnetic Energy Storage, Dynamic voltage restorer, voltage sag, modular multilevel converter.

1. INTRODUCTION

The enhancement of energy top quality is an important objective for electrical resources and commercial and commercial consumers. Highly sporadic allocated generation, rapidly changing plenty, and direct-off-line energy electronic systems all contribute to reduced energy top quality causing equipment down time, overload and failure leading to lost revenue [1]. Voltage interference is a prevalent problem and under-voltage conditions have been seen to happen more regularly than overvoltage circumstances [2]. Short-term under-voltage sags are described in IEEE Std. 1159-1995 [3] as a reduce to between 0.1 and 0.9 p.u. (per unit) r.m.s voltage for time periods of 0.5 cycles to 1 min. They happen more, long-term under-voltages with important costs to market [4]. Long-term under-voltage activities are described as a calculated voltage less than 0.8-0.9 p.u. r.m.s voltage, staying longer than 60 seconds or so [3] and can lead to fill losing and possibly to voltage failure [5]. The research below provides a means by which both short-term and long-term voltage variations can be reduced at the fill using short-term attractive power storage space and long-term battery energy storage space.

As the primary portion of DVR, the VSI has various topologies: two-level [6-7] or multilevel converters [8, 9]. Due to the top dv/dt, the conventional two-level converters have great changing failures and high frequency harmonics. And a heavy narrow is needed between the ripper and the treating transformer. A lot of research and accomplishment on multilevel-converter-based DVR have been designed, such as the cascaded H-bridge (CHB) [9] and modular multilevel ripper (MMC or M2C) [10]. The multilevel-DVR, consisting by capacitors and IGBTs with low voltage ranking, can be used for medium-/high-voltage mitigation programs with low changing failures and harmonics. Thus heavy filtration is not needed. Nevertheless, a challenging trouble in the multilevel converters is the capacitor voltage controlling management, which is revealed in many literatures [11-16]. This paper suggests a parallel-connected diode-clamped to be used in DVR. The new topology, derived from the general multilevel converter and the diode-clamped with energy evaluations routine can recognize capacitor voltage stability instantly without any management techniques or reviews.

Low energy ranking clamping diodes and inductors are used to management the capacitor currents. Along with this topology the voltage compensation method also created.

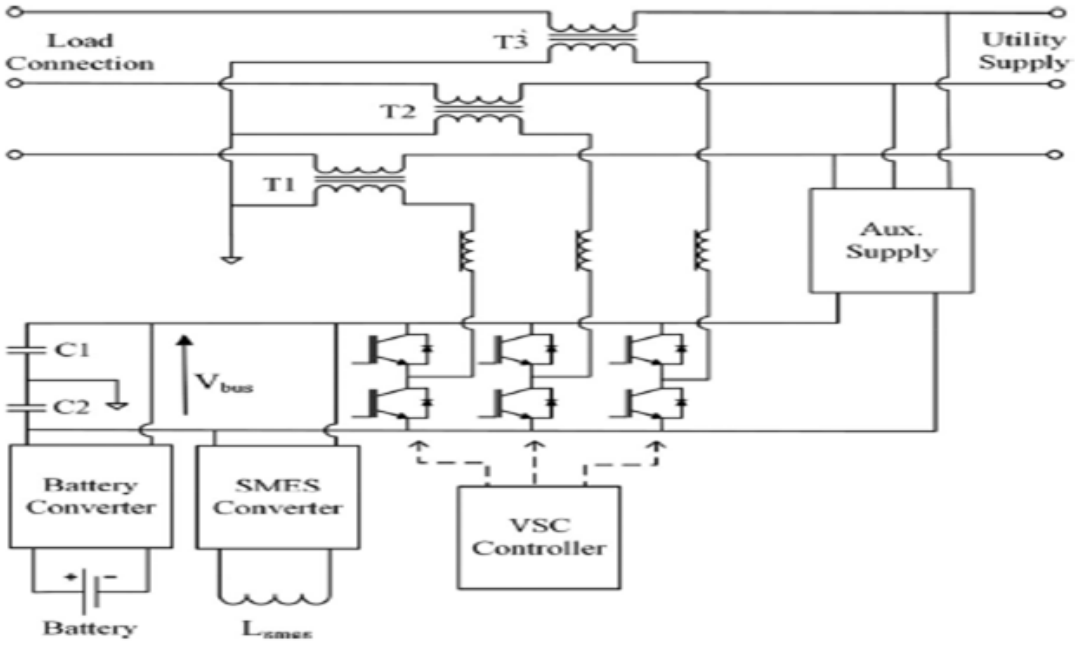

Fig.1: Hybrid Energy DVR system configuration

Fig. 1 reveals the DVR system considered. The SMES has been emulated by a 15 mH, 100 A inductor. During a voltage miscalculation a three-phase inverter is used to produce the settlement volts at the main of the injection transformers (T1-T3) so that the load volts continue to be near to affordable. DC/DC converters are used to interface battery energy and SMES-emulator to the DC bus. A reliable offer (Aux. Supply) is used to back up the DC bus during stand by function and cost the energy storage devices. [17-21].The reliable offer is turned off and the energy storage gadgets deliver the necessary energy for the inverter to support the burden during a volts mistake.

2. SMES-EMULATOR AND BATTERY SYSTEM

To reduce cost and be able to examine a SMES-battery hybrid DVR management system, the SMES system was replicated by using a 15 mH iron-core inductor in this research. The SMES converter was in accordance with the asymmetric H-bridge settings shown in Fig. 2. This converter was rated at up to 220 A continuous current using pressured air chilling. During charge, Q2 takes place ON and Q1 is modulated whereas during discharge Q1 takes place off and Q2 is modulated. The link between DC bus present, inductor present and responsibility rate, is given by (1) and (2) for charge and discharge[22].

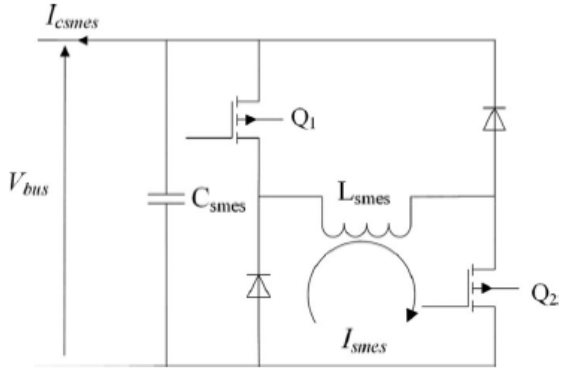

Fig 2: SMES DC/DC converter

$$I_{csmes}=(V_{bus}-V_{nom\_smes})k_{smes} \text{ -------(1)}$$

where k_{smes} is the gradient of the droop controller and V_{nom_smes} is the nominal voltage of the droop controller.

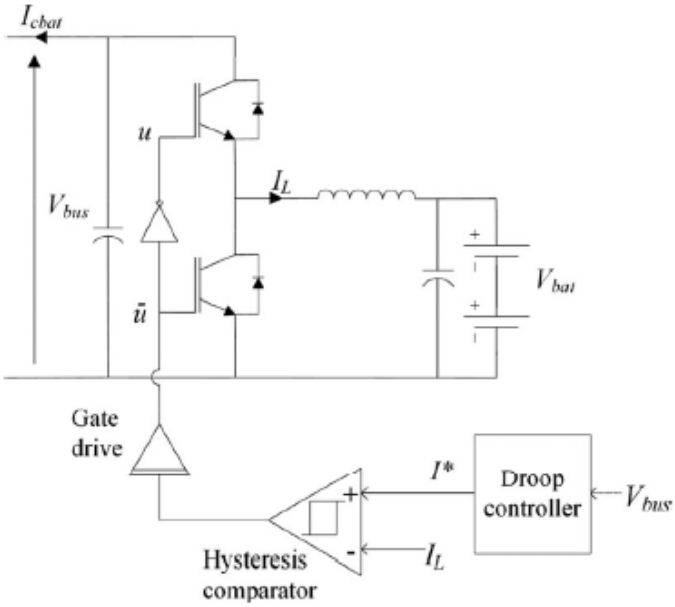

Fig 3: Battery DC –DC converter

Fig. 3 reveals A bidirectional synchronous-buck coverter with a rating of 40 A output current with hysteresis present management was used to control battery. This topology has been formerly revealed for use with interfacing an ultra-capacitor power space for storage program to the DC bus in DVR program. However, the proposed system varies from past research in that a varying frequency
hysteresis present management has been used. This is advantageous as it functions cycle-by-cycle present restricting, making it resistant to short circuit faults.

$$L\frac{diL}{dt} = V_{bus}\,u - V_{bat}\,u' \text{--------(2)}$$

Where u is a gate drive signal and V_{bat} and V_{bus} are battery and DC bus voltages. To achieve active current droop control, the inductor current reference $I*$ is set as follows:

$$I* = (V_{bus} - V_{nom\_bat})\,k_{bat}\frac{V_{bus}}{V_{bias}} \text{ ----- (3)}$$

3. CONFIGURATION OF THE DVR

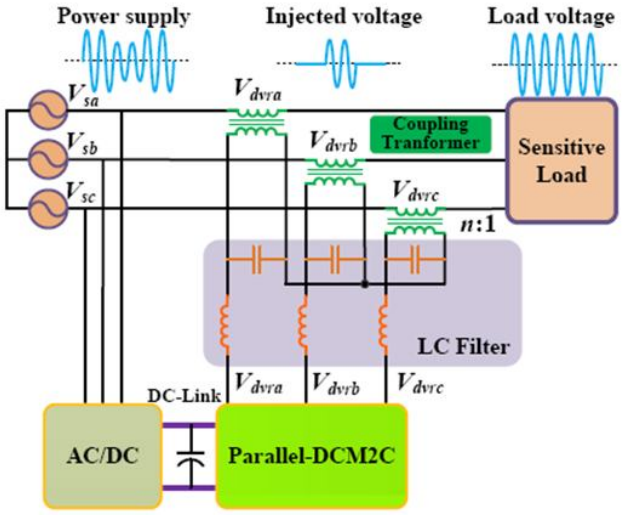

Fig 4: Scheme of DVR system

The scheme of DVR system is shown in Fig. 4. The energy resource currents are V_{sj}, j = a, b, c. The DC link voltage of the suggested parallel-DC flip multilevel ripper is offered by an AC/DC ripper. The outcome currents of the ripper, V_{dvrj}, are treated to the lines through three combining transformers in which the changes rate is n : 1. Output filtration are essential to remove the high regularity harmonics. Due to the multilevel voltage features, the narrow quantity has a more compact footprint than that used in conventional two-level converters. The injected voltage is in series with the source voltage, so the load voltage can meet the required waveforms.

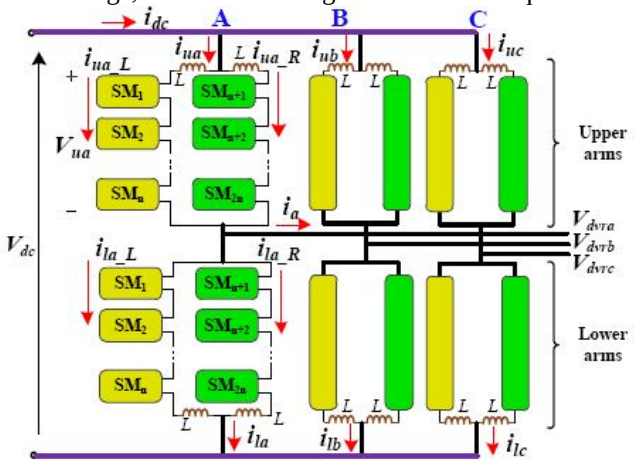

Fig 5: Three phase structure of parallel-DCM2C

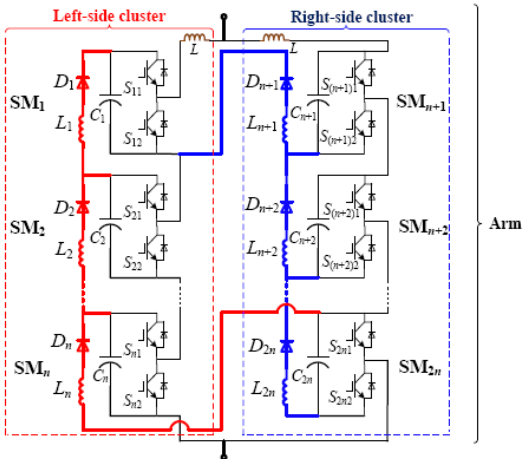

Fig 6: One arm structure

Fig. 5 shows the topology of the suggested identical DCM2C. Just like conventional M2C with two-star framework, the suggested converter comprises of 6 arms. Each arm has two groups, the left-side group and the right-side group, which are linked in identical. Each group contains one narrow inductance and n SMs. The particular relationship routine of the arm is showed in Fig. 6. Evaluating to M2C topology, the additional clamping diode and inductor are set up in each SM to help the capacitor voltage stability.

4. OPERATION PRINCIPLES

A. CAPACITOR VOLTAGE BALANCING PRINCIPLE

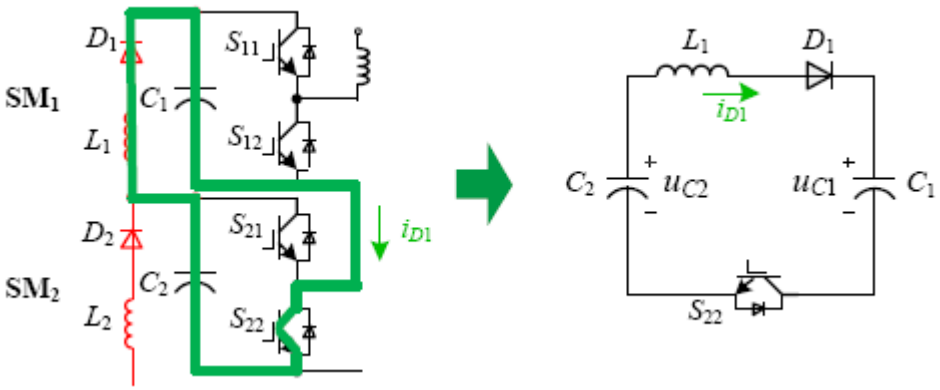

Fig. 7: Simplified circuit of SM1 and SM2

Assume that the power switches and clamping diodes are ideal, which indicates there are no volts falls across the devices when they are kept on condition. To be able to evaluate the clamping procedure, simplified circuits of SM1 and SM2 is derived in Fig. 7, then the following two situations are need to be discussed:

Case a: If the voltage of C1 is larger than or equal to that of C2, namely uC1 ≥ uC2, no current is generated in this clamping circuit. The relation of the two voltages remains unchanged.

Case b: If the voltage of C1 is lower than that of C2, namely uC1 < uC2, balancing current, iD1, will occur and flows from C2 to C1.

B. VOLTAGE MITIGATION

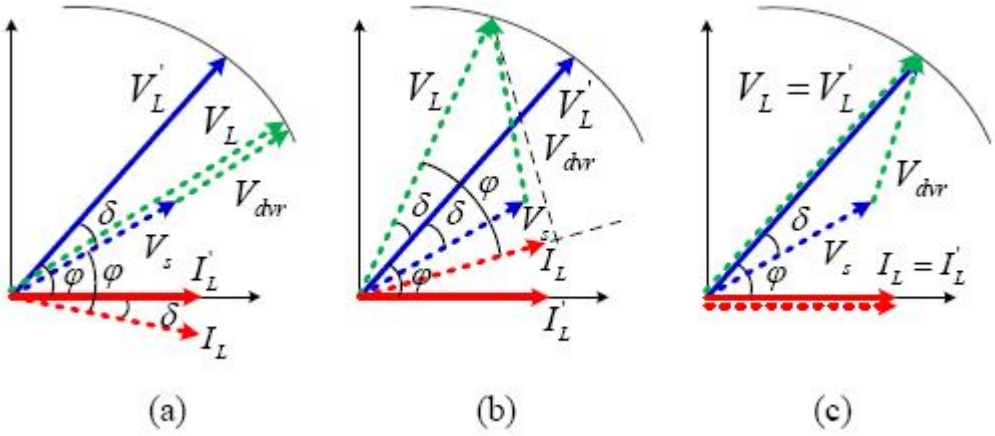

Fig. 8: Phasor representations of the three basic strategies: (a) in-phase; (b) energy-optimized; (c) pre-sag.

The DVR minimization program has been revealed in many literatures. Three primary techniques, the pre-sag settlement, in-phase settlement and energy-optimized settlement are shown in Fig. 8. The V_L' and I_L' signify the load voltage and current before voltage sag, respectively. VL and IL are the grid volts and load current after settlement, while Vs and V_{dvr} are the grid voltage and injected voltage. φ is the power factor of the load.

(a) In the in-phase compensation method, the DVR injects the smallest voltage magnitude, and the phase angle is synchronized to the sag gird voltage. Thus, if a phase jump δ occurs, it cannot be corrected in this method, and the load tripping may appear.

(b) In the energy-optimized compensation method, the DVR injects as little active power as possible to the load to compensate the sag voltage, aiming to prolong the compensation time with limited energy storage system. If the voltage sag is shallow, as shown in (6), this method can compensate the voltage with only reactive power. Hence the compensation time will be infinite theoretically. But the phase jump still cannot be correct.

(c) In the pre-sag compensation method, both the phase jump and voltage sag can be corrected. A large amount of active power needs to be injected into the grid even during shallow voltage sag. This method can provide the best voltage performance for the load.

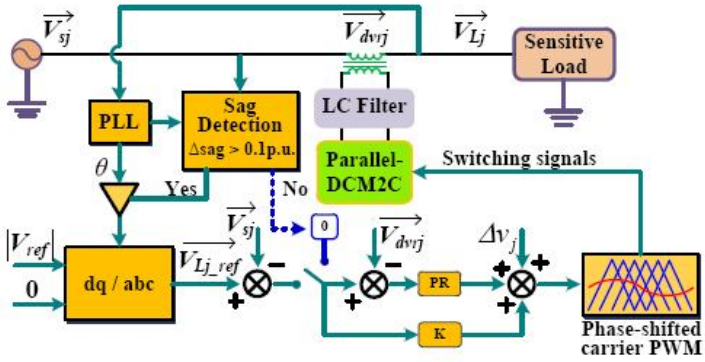

Fig. 9: Control block of the proposed DVR system.

In this paper, having to the support of the AC/DC system and the multilevel converter, the pre-sag compensation method is used. The control block is shown in Fig. 9.

The sag detection is implemented by

$$\Delta sag = \sqrt{Vref^2 - (Vd^2 + Vq^2)} \quad \text{----- (4)}$$

Here Vref is the referrals volts of the load. Vd and Vq are the grid voltage in d-q axis elements respectively, and the required phase angle in the modification is from the load voltage. In regular situation the Δsag is lower than 0.1p.u. and they handled voltage is zero; Once the Δsag is bigger than 0.1p.u., the DVR begins to compensate. The load voltage phase angle θ will be replaced into the d-q modification. The output, V_{Lj}_ref , is the referrals vector of the load. Thus the phase angle jump will be prevented. Mixture of feedback and feedforward control is used on the injected voltage. The current-sharing control outputs, ΔVj, are included to the outputs of compensation controller, and the sum consists the modulation signals.

5. RESULTS

In order to verify the performance of the proposed DVR, a hardware prototype was constructed. The battery was a 48 V, 75 Ah sealed lead acid type and the SMES-emulator was 15 mH/100 A iron-core inductor. The nominal AC bus voltage was set to 120 Vac using a step down transformer. The load was configured as a 1.4 kW star-connected resistor.

Initially a three-phase voltage sag to 35% of nominal voltage, lasting 100 ms was used to demonstrate the response of the DVR and energy storage systems. From Fig. 10 it can be seen that the hybrid DVR system mitigates the voltage sag effectively during the sag event. The battery is discharged momentarily at −1.45 A at the end of the sag when the inductor energy has been depleted.

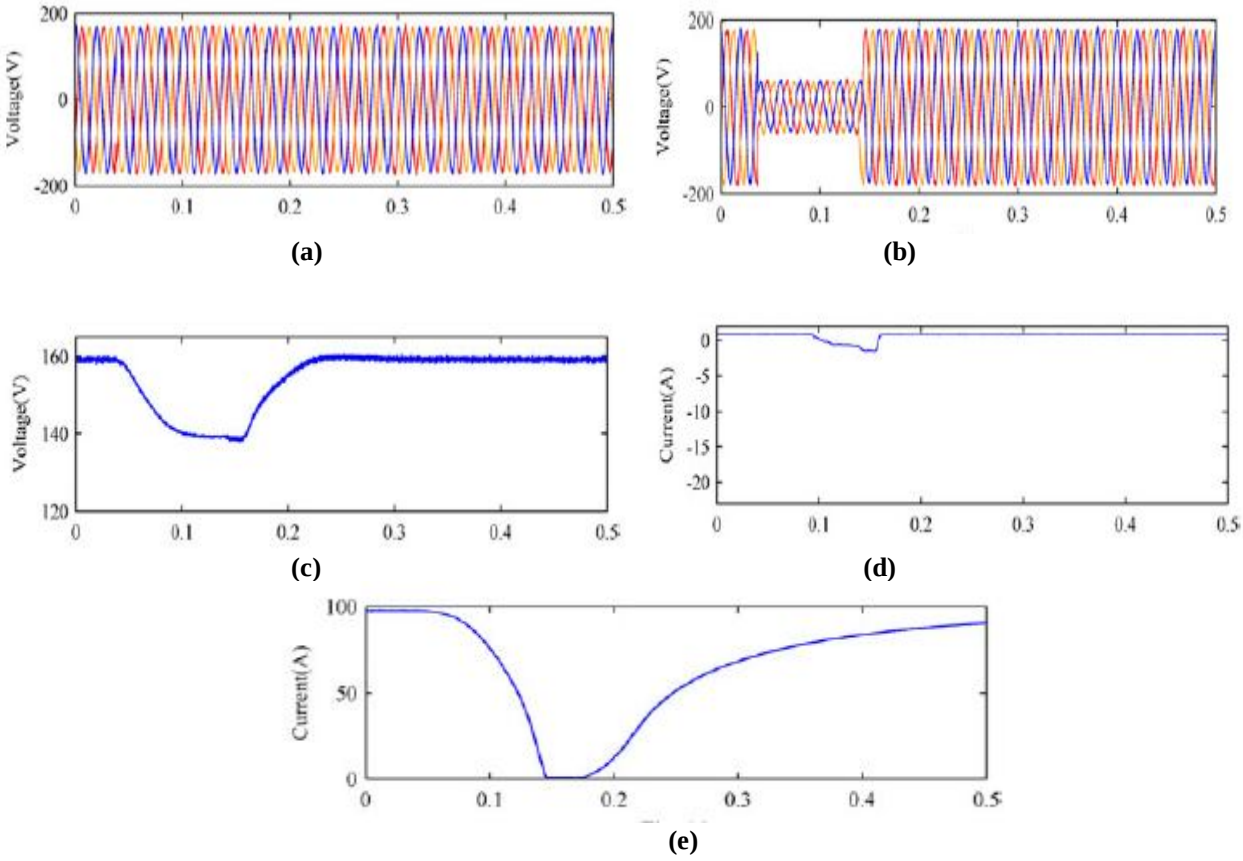

Fig. 10: Hybrid System Experimental results: 0.1s Three phase sag to 35% of nominal voltage. (a) Supply voltages.
(b) Load voltages (c) DC Link Voltage Battery Current (e) SMES-inductor current.

The SMES-emulator was then removed from the system and the test was repeated. The system response to the same threephase
sag with only battery energy storage is shown in Fig. 11. As the DC bus voltage falls below 140 Vdc (the battery system nominal voltage) the battery is discharged to support the DC bus. The peak battery current is 21.13 A in this case and the DVR system can be seen to effectively mitigate the voltage sag [23, 24, 25].

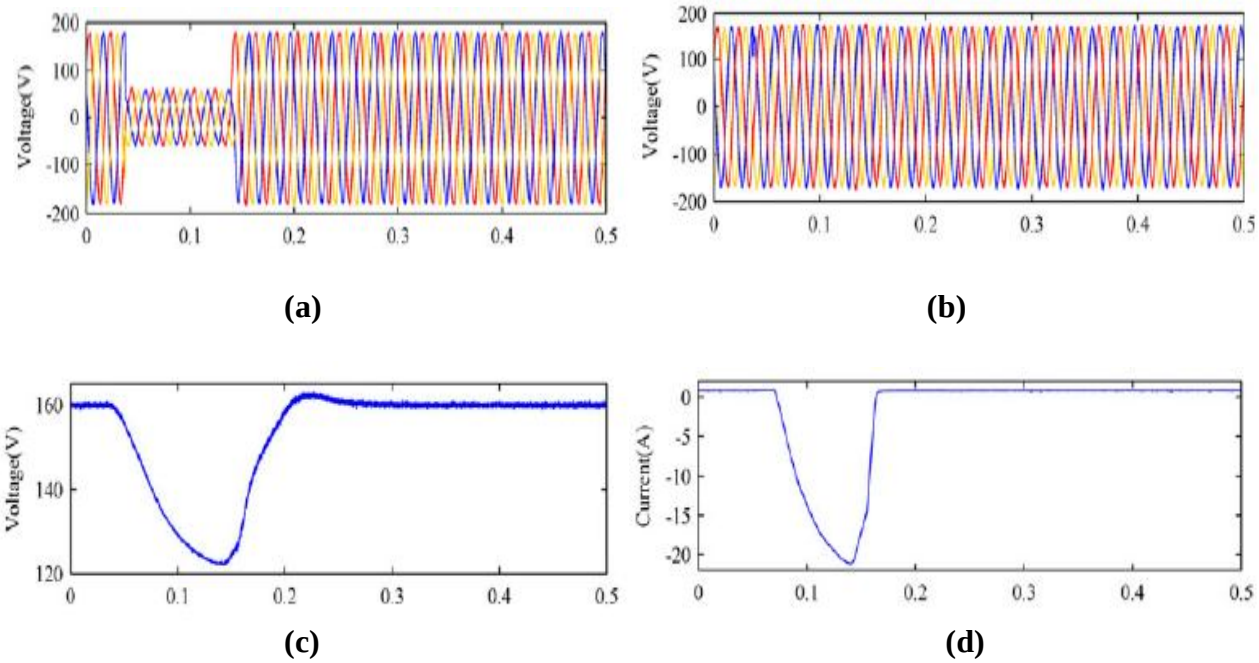

Fig. 11. Battery System Experimental results: 0.1s Three phase sag to 35% of nominal voltage. (a) Supply voltages (b) Load voltages (c) DC Link Voltage (d) Battery Current.

Fig. 12 shows the capacitor voltages from the left- and right-side clusters of upper arm during voltage compensation. The voltage deviations are very small, basically smaller than 1V. This result verifies the excellent performance of the clamping diodes in regulating the capacitor voltages.

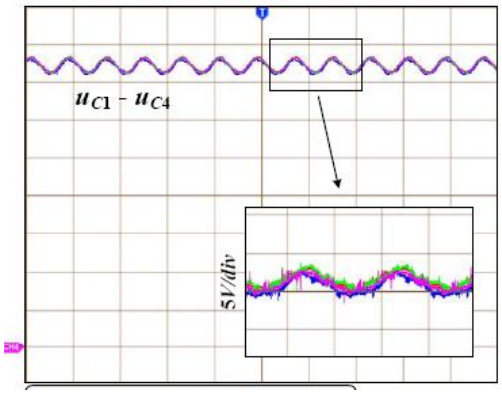

Fig. 12: Experimental waveforms of the capacitor voltages in upper arm of the parallel-DCM2C.

Fig. 13 shows the currents flowing through the arm, and the left-/rightside cluster are shown in. The good distributing performance in the two clusters verifies the effectiveness of the proposed current-sharing control.

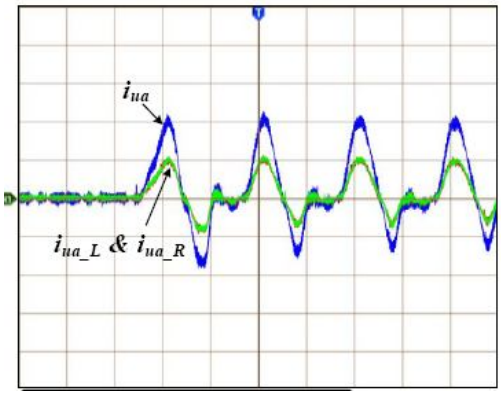

Fig. 13:. Experimental waveforms of the currents flowing through the left- and right-side cluster, and the whole arm.

6. CONCLUSIONS

The system has been shown to autonomously prioritise the use of the short-term energy storage system to support the load during deep, short-term voltage sags and a battery for lower depth, long-term under-voltages. This can have benefits in terms of improved voltage support capability and reduced costs compared with a SMES-based system. Additional benefits include reduced battery power rating requirement and an expected improvement in battery life compared with a battery-only system due to reduced battery power cycling and peak discharge power. A new DVR system based on the parallel-DCM2C, in which clamping circuits are applied to keep the capacitor voltages balanced. Comparing to traditional MMC, no balancing control algorithms or SM voltage sensors are needed in the proposed converter. Although extra diodes and inductors are required to clamp the capacitor voltages, the low current rating electrical characteristics will help to reduce the size and cost of the clamping circuits. With the developed pre-sag compensation method, the parallel-DCM2C can restore the load voltage both in phase angle and amplitude.

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