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Electrical Characterization of Al/n-CdTe/NiCr Schottky Diodes

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ABSTRACT

Schottky barriers of Al /n-CdTe/ NiCr structures have been prepared and was studied. The films were prepared by thermal evaporation with different thicknesses (400, 600 and 1000) nm at 273Kand annealed at 373K and 473K through 30 min. Schottky barrier characteristics (J-V) and (C-V) have showed that the rectification properties and barrier height increases with the increasing thickness and annealing temperatures, while saturation current density and the ideality factor was decreased. Photovoltaic effect of these junctions was very poor and fill factor relatively low. high defect density, presence of an interfacial layer, low doping concentration are perceived to affect the J–V characteristic.

Keywords:- Schottky barrier junction; I-V characteristics; C-V characteristics; Solar cell.

1. INTRODUCTION

In recent years, the study of binary elements compounds was increased in order to find new materials for solar cells. Scientific research has focused on solar cells composed by thin films in order to obtain a high efficiency with relatively low cost. Thin-film composed of the elements of columns 2-6 have been used in the periodic table in many semiconductor devices such as photo-electrochemical ,filed effect transistors, detectors, photodiodes, photoconductors and photo voltaic solar cells[1]-[2] .

Among the elements of columns 2-6 of atomic table was Cadmium Telluride CdTe of the most promising materials in the production of thin films used in CdTe hetrojunction and metal - CdTe Schottky barriers due to the direct band gap about 1.47 eV near the optimum value for the effective conversion of solar energy at room temperature, and it is a good absorber for sunlight with high optical absorption coefficient ($\alpha > 10^4 cm^{-1}$)[3] . There are a variety of methods have been employed to prepare CdTe films and their junctions with metal, the most important vacuum evaporation[4] , rf sputtering [5]. , and molecular beam epitaxy[6].The vacuum evaporation method has some advantages such as: the amount of impurities included in the growing layer which will be minimized, the tendency to form oxides which will be considerably reduced and finally straight line propagation which will occur from the source to substrate [1]. For this, in the present paper we use thermal evaporation technique to prepare the Al /n-CdTe/ NiCr Schottky barriers diode with different thickness and annealed at 373Kand 473K through 30 min. The electrical characteristics of this device are studied in the dark or under illumination.

2. EXPERIMENTAL

In this work we have prepared Al/CdTe/NiCr structures by using CdTe (99.99% pure) (n-type) with Electron affinity (4.4eV) as a semiconductor substrate and we choose the (Al) with work function (4.13 eV) as ohmic contact and NiCr with work function (5.56 eV) as Schottky contact.

First we cleaned glass substrates of dimension (25.4x76.2)mm by using soap-free detergent and followed by multiple rinsing in boiling water then rinsing in distilled water to remove traces of detergent, and then the substrates were cleaned in an ultrasonic cleaner for 15 min with ethanol. The last step of clean was drying the substrates.

The layers of aluminum were deposited by thermal vacuum evaporation using Balzer's coating unit model (BL 510) at pressure less than 10^{-5} mbar on glass substrate with a thickness 200nm. The evaporation process was performed in vacuum enclosure which provided with the necessary arrangements like evaporation source (Mo boat), movable substrate holder and radiant heater, were fixed inside the chamber. CdTe film was also grown by thermal evaporation method (Edward 306) at 300k with thickness of the order(t=400 nm , 600nm and 1000nm) done by using vacuum system model.The Schottky barriers were prepared by vacuum evaporation of nickel-chromium on front side of the CdTe with a thickness 40 nm. after that we annealed the samples under (Ta=375K, 437 K) at (10^{-5} Torr) pressure in

vacuum for (30 min). The equipment for measuring J-V consisted of a Keithley 616 digital electrometer, power supply 1540D.C 40-300A, Philips Multimeter with 10^{-14} resolution.
(J-V) characteristics of Al/CdTe/NiCr Junction in reverse and forward bias in dark was made by D.C power supply and two digital electrometers type Keithly. The junction was illuminated using Halogen lamp type Philips (120W) with different intensities (45, 105) mW/cm^2. The capacitance of Al/CdTe/ NiCr structures were measured as a function of applied reverse bias voltage between -1 to 1.5 Volt with frequency 100KHz by using HP-R2C unit model 4274A and 4275A multi-frequency LRC meter.

3. RESULTS AND DISCUSSION

3.1 Current density- Voltage Characteristics of Schottky barrier

Figure (1) shows (ln J-V) characteristic for Al/CdTe/NiCr Schottky junction at forward and reverse bias voltage in dark as deposited and for different annealing temperatures and thickness. In general, the relationship between the applied-bias voltage and the current through a barrier between metal and semiconductor of the MS, MIS and solar cells, based on thermionic emission theory (TE), is given by[7]-[8] :

$$J = J_s exp\left(\frac{qV}{nk_BT}\right)\left[1 - exp\left(\frac{-qV}{k_BT}\right)\right] \qquad (1)$$

where V is the applied bias voltage on the Schottky Barrier Diode (SBD), n is an ideality factor and I_s is the reverse saturation current derived from the straight-line intercept of Ln(J) at zero bias is given by :

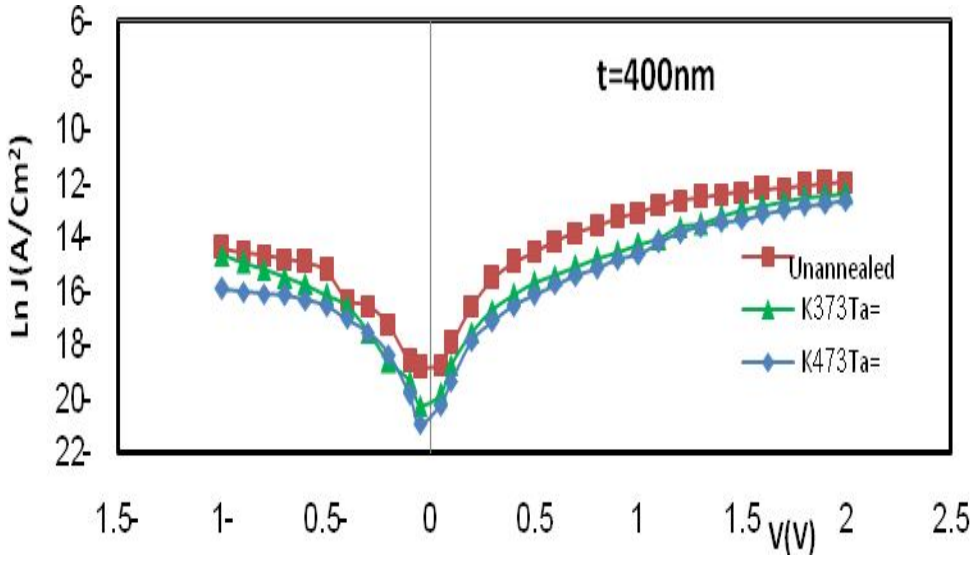
$$J_s = A^* exp\left[\frac{-q\varphi_B}{k_BT}\right] \qquad (2)$$

where Φ_B is the zero-bias barrier height, A is the rectifier contact area,A^* is the effective Richardson constant and equals to 12 A cm^{-2} K^{-2} for n-type CdTe, T is the absolute temperature in Kelvin and k_B is the Boltzmann constant. The ideality factor is calculated from the slope of the linear region of the forward bias LnJ-V plot and can be written from Eq.(1) as :

$$n = \frac{q}{k_BT}\left(\frac{dV}{dLnJ}\right) \qquad (3)$$

where dLnJ/dV is the slope of linear region of Ln(J) vs V plots.
The value of Φ_B is calculated from the extrapolated J_s at zero according to following equation as :

$$\Phi_B = \frac{k_BT}{q} ln\left(\frac{A^*T^2}{J_s}\right) \qquad (4)$$



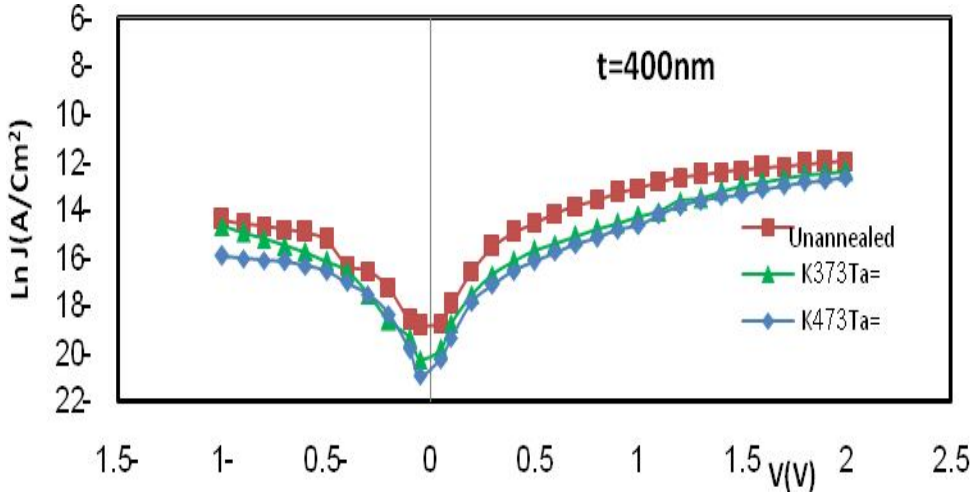


Figure (1): Ln J-V characteristic for Al/*n*-CdTe/ NiCr at forward and reverse bias voltage at different thicknesses and annealing temperatures.

From table (1) , we find that the values of ideality factor (n) for Al/*n*- CdTe /NiCr SBD_s is considerably larger than unity. The high value of ideality factor indicates that the junctions were non-ideal and most of the carriers (of electrons and holes) recombine at the junction (depletion) region, tunneling effect are the main reasons. On the other hand, there can be many reasons to get junction ideality factor greater than unity; Henish [9]. attributed this to the presence of an interfacial layer, image force lowering of barrier height, Sarmah and Rahman [5] attributed to the presence of an interfacial layer and tunneling effect. Bayhan and Erecelebi [10]. attributed to the increase of (n) to the series resistance effects which are associated with the neutral region of the semiconductor (between depletion layer and ohmic contact). Also it can be found the value of n and J_s decrease with increasing annealing temperature and thickness and that is may be due to increase the junction resistance. Similar results have been reported by Chen [11].

Furthermore, it can be seen from table (1) that there is an increase in the barrier height with the increase of the annealing temperatures and increase semiconductor thickness. These results may be attributed to the reduced surface state and dislocation at interface layer. Also it can be noted that the values of Φ_B deviate from the expected value and the cause for this, is thin oxide layer formed between metal and semiconductor on exposure to atmosphere has been reported to influence the barrier height. This layer may be considered to be an insulator, even though it may be so thin that it does not possess the band structure which is the characteristic of thick oxide. Because of the potential drop in the oxide layer, the barrier height will be lower than it would be in an ideal diode. Similar behavior has found by Lalinski et al [12]

Table (1): J-V characteristics for Al /*n*-CdTe/ NiCr at different thicknesses and annealing temperatures.

sample	t (nm)	T_a(K)	J_s(A/Cm^2)	n	Φ_B(eV)
Al/CdTe/ NiCr	400	un annealed	$8x10^{-9}$	3.5	0.81
		373	$5x10^{-9}$	3.3	0.825
		473	$2x10^{-9}$	3.01	0.848
	600	un annealed	$3x10^{-9}$	3.3	0.837
		373	$1x10^{-9}$	3.1	0.86
		473	$0.8 x10^{-9}$	2.9	0.87
	1000	un annealed	$0.5 x10^{-9}$	2.4	0.88
		373	$0.2 x10^{-9}$	2.2	0.9
		473	$0.1 x10^{-9}$	2.05	0.92

3.2 Capacitance-Voltage (C-V) Characteristics

The barrier height can also be determined by capacitance measurement. In this method the diode capacitance is measured as a function of applied reverse bias.

For a metal *n*-type semiconductor Schottky diode, C–V measurements yield the donor net concentration N_D and the value of built-in voltage V_{bi}. The relation between capacitance and voltage is given by [7]:

$$\frac{1}{C^2} = \frac{2(V_{bi} + V)}{A^2 \varepsilon_S \varepsilon_\circ q N_D} \qquad (5)$$

Where,
ε_S : is the semiconductor permittivity
$\varepsilon_\circ$: is the permittivity in vacuum.

The slope of the $1/C^2$ against V plot reveals N_D whereas V_{bi} can be obtained from the intersection between the $1/C^2$ line and voltage axis.

The Schottky barrier height and built-in voltage are interrelated [7]:

$$\Phi_B = V_{bi} + V_n + \frac{k_B T}{q} \qquad (6)$$

With Vn the distance between the bottom of conduction band and Fermi level given by following equations:

$$V_n = \frac{k_B T}{q} \ln \frac{N_C}{N_D} \qquad (7)$$

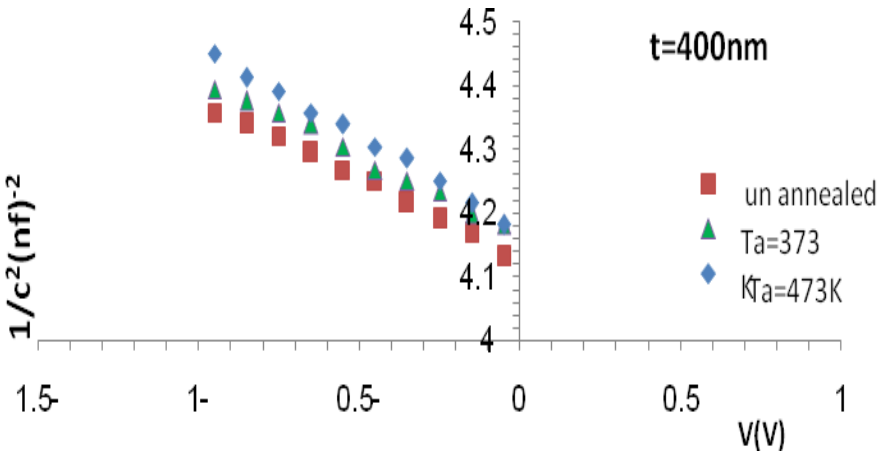
With

$$N_c = 2\left(\frac{2\pi m^* k_B T}{h^2}\right)^{\frac{3}{2}} \qquad (8)$$

Where,
m^* : is the density of states effective mass for electrons, in case of CdTe it is 0.10 m_o.
N_C: is the effective density of states at the bottom of conduction band.
Equations (6) and (8) allow to calculate Φ_B once N_D and V_{bi} are known.

The square of inverse capacitance is plotted against applied reverse bias voltage in the range of (0-1) Volt at frequency equal to 1 MH_z at room temperature has been studied for Al /*n*- CdTe / NiCr diodes at different thicknesses , and annealing temperature are shown in figures (2) . The interception of the straight line with the voltage axis at ($1/C^2 = 0$), represents the built – in voltage. It can be observed from table (2) that the built–in voltage increases with increasing semiconductor thickness , and annealing temperature as a result of the decrease in the capacitance value and the increase of the depletion width. From the same table, it can be noted that the decreasing in doping concentration N_D which lead to increase of the depletion width and decrease the capacitance. As the doping concentration is moderate, the current transport is assumed to be mainly dominated by the thermionic emission process[7]. Also, it can be observed that the barrier heights Φ_B obtained from the C–V measurements are comparatively larger than the obtained values from J–V. The barrier heights obtained from the J–V measurements are more meaningful for assessing the diode performance as the interface traps neither respond to applied Ac signals nor contribute to capacitance at higher frequencies.

The effects of an insulating layer or charges existing at the semiconductor-metal interface must be considered. Most Schottky diodes have a thin oxide or insulating layer at the metal-semiconductor junction unless all the processing is done in a vacuum.



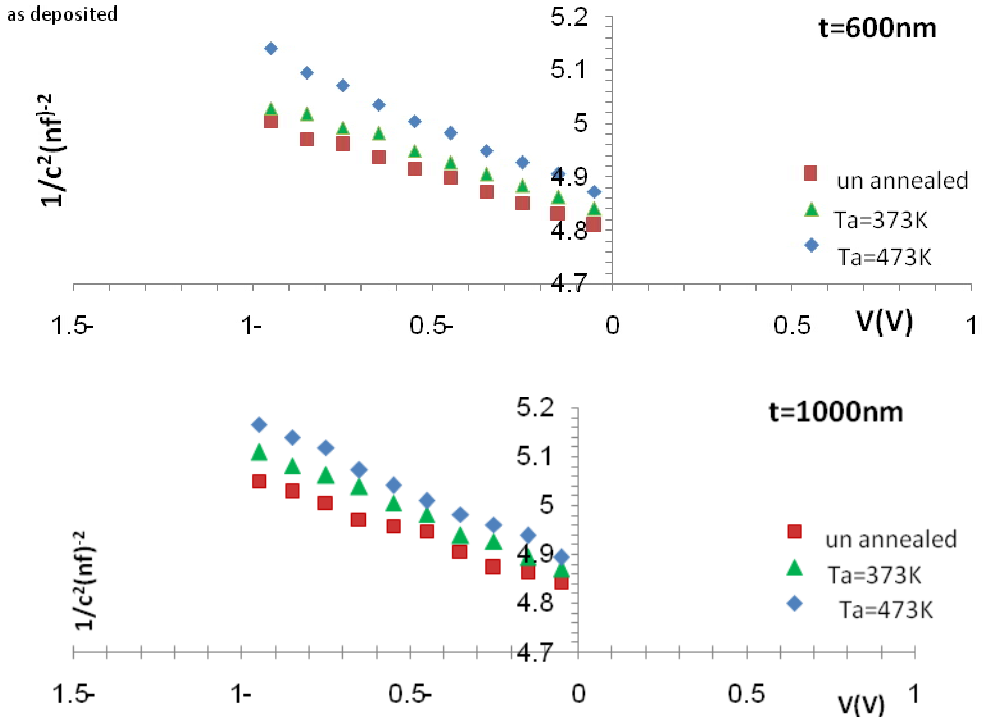


Figure (2): Inverse capacitance vs reverse bias voltage for Al/n-CdTe/NiCr at different thicknesses and annealing temperatures

Table (2): C-V characteristics parameters for Al /*n*-CdTe/ NiCr at different thicknesses and annealing temperatures.

Sample	t (nm)	Ta(K)	$N_D(cm^{-3})$	V_{bi} (V)	Φ_B(eV)
Al/CdTe/NiCr	400	un annealed	$4.1x10^{16}$	0.79	0.873
		373	$3.9x10^{16}$	0.80	0.884
		473	$3.5x10^{16}$	0.82	0.9
	600	un annealed	$3.69\ x10^{16}$	0.81	0.891
		373	$2.77\ x10^{16}$	0.82	0.91
		473	$2.31\ x10^{16}$	0.85	0.937
	1000	un annealed	$3.36\ x10^{16}$	0.85	0.93
		373	$2.64\ x10^{16}$	0.87	0.955
		473	$2.21\ x10^{16}$	0.89	0.98

3.1 Short Circuit Current, Open Circuit Voltage and Efficiency Measurement for Schottky Barrier Solar Cells.
The Schottky barrier junctions were studied for their photovoltaic performance under the light intensity of 45 mW/ cm^2 and 105 mW/cm^2.
Figures (3(a,b)) show current density–voltage curves of Al /n- CdTe / NiCr schottky diodes at different thicknesses, and annealing temperature under different light power for photovoltaic effect.
Low photovoltage has been observed in these junctions. Since the counter electrode was not made too thin to allow the whole light to penetrate through it, a minute fraction of it absorbed at the surface is not ruled out.
Table (3) show the open circuit voltage, short circuit current, fill factor and efficiency of a these samples. There are various factors responsible for the reduction in the photovoltage such as high defect density, presence of an interfacial layer, low doping concentration and presence of series resistance. Low photovoltage in CdTe Schottky barriers has also been reported by Das *et al.* [13].
Also, it can be seen from the same tables that increasing J_{sc} and V_{oc} directly with: thickness, annealing temperature and power density for Al/CdTe/NiCr Schottky barrier solar cells.

This manner of proportionality is attributed to the increasing in the grain size and reducing the grain boundaries and improvement of structure which leads to the increase of the mobility and increase the photocurrent as well as the increase of the depletion width which leads to an increase of the creation of electron-hole pairs.
From increasing of J_{sc} and V_{oc} with increasing the thickness and annealing temperature the efficiency η **%** increased directly with both thickness and annealing temperature for Al/CdTe/NiCr Schottky barrier solar cells.

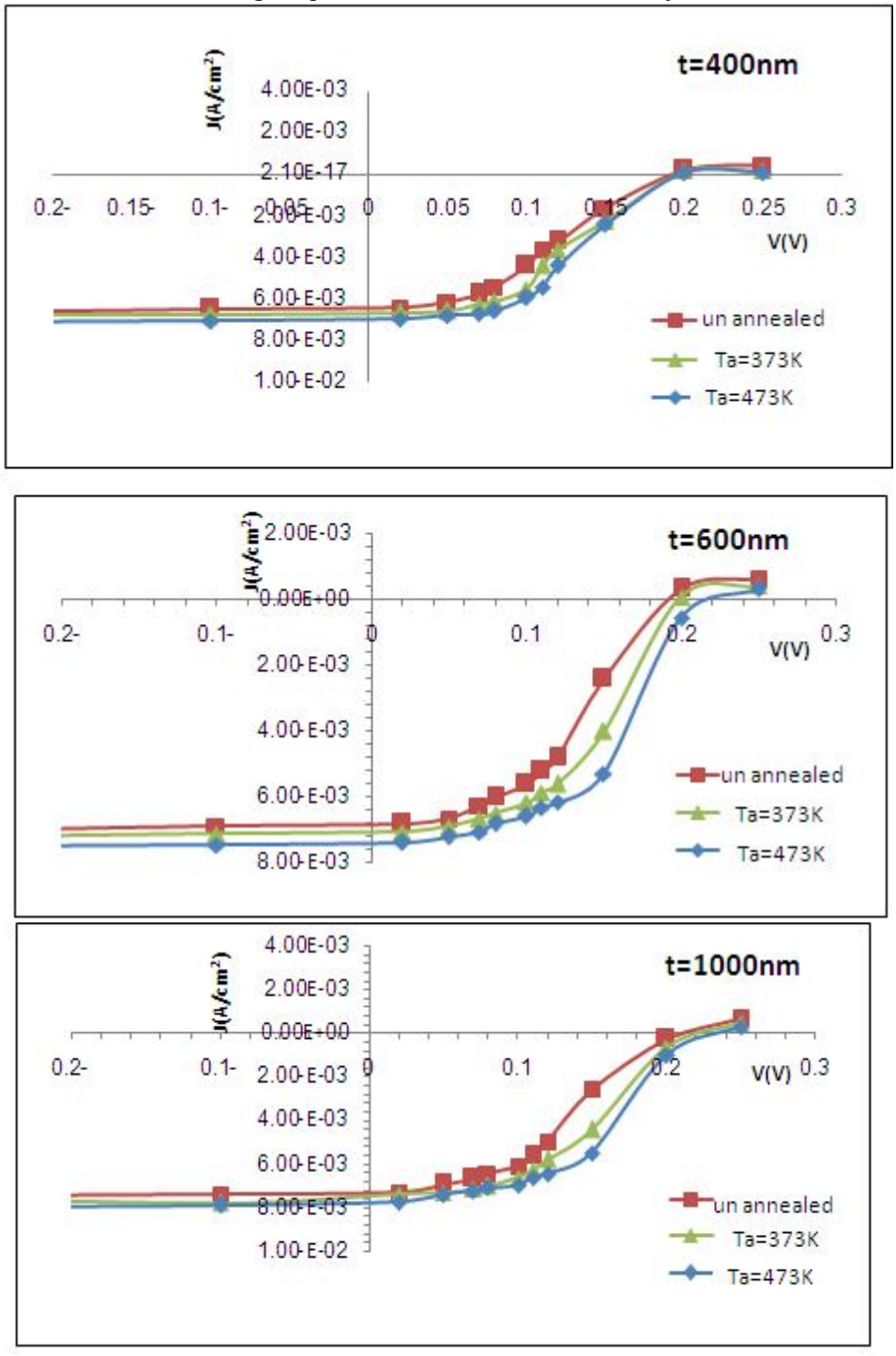


Figure (3(a)) J-V characteristic for Al/*n*-CdTe/NiCr at different thicknesses and annealing temperatures under light power=45mW/cm^2

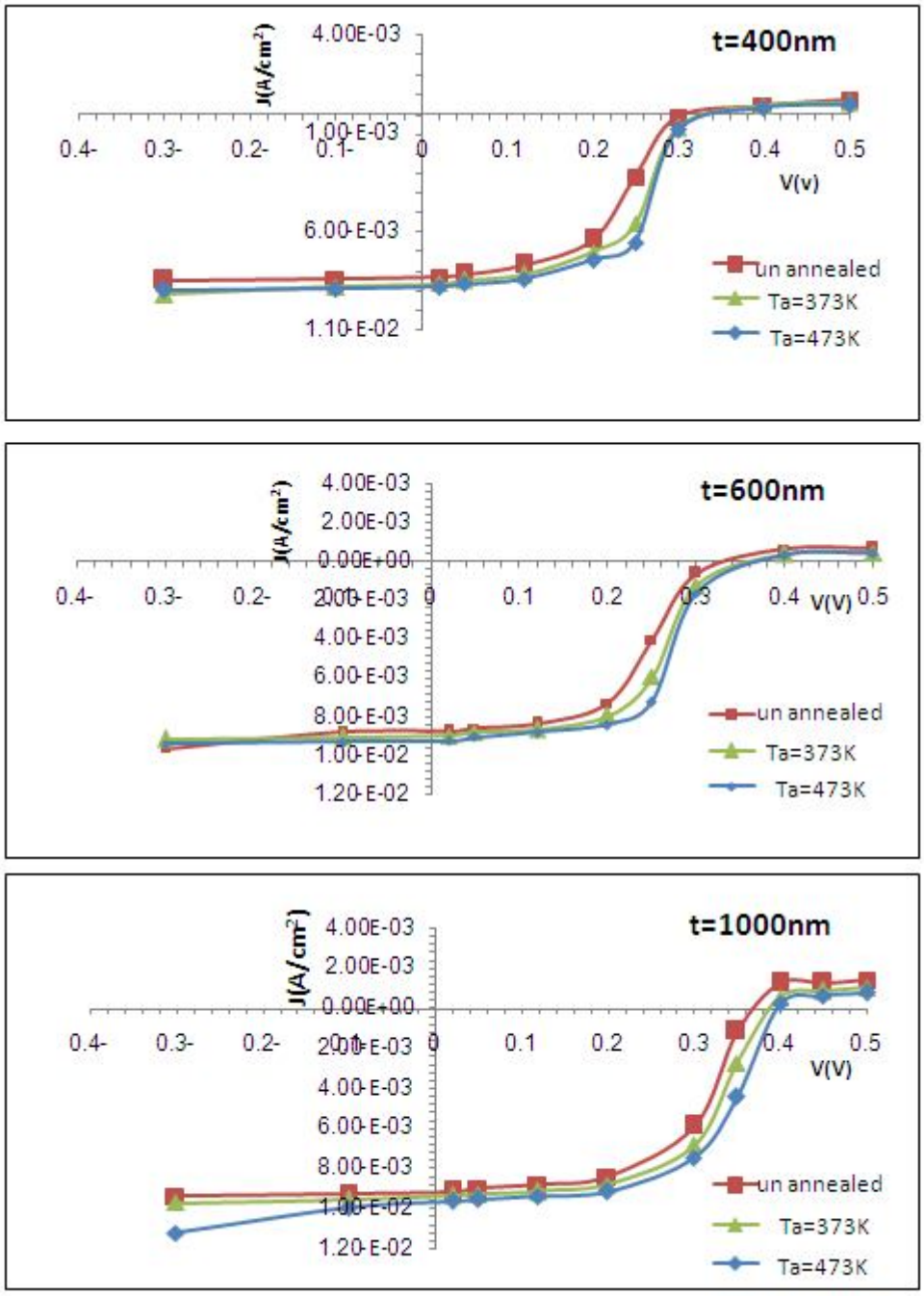


Figure (3 (b)) J-V characteristic for Al/*n*-CdTe/NiCr at different thicknesses and annealing temperatures under light power=105mW/cm^2

Table (3): The current density –voltage parameters for Al /CdTe/ NiCr Schottky solar cell for different thickness and annealing temperatures

Illuminated Under Light Power =45 mW/cm^2							
t(nm)	**T_a(K)**	**V_{oc}(V)**	**J_{sc} (mA/cm^2)**	**V_{max} (V)**	**J_{max} (mA/cm^2)**	**F.F**	**η %**
400	un annealed	0.18	6.5	0.095	5.1	0.4141	1.07
	373	0.19	6.7	0.1	5.3	0.4163	1.17
	473	0.195	6.8	0.105	5.35	0.4236	1.24
600	un annealed	0.19	7	0.105	5.4	0.4263	1.26
	373	0.21	7.3	0.12	5.5	0.4305	1.46
	473	0.215	7.4	0.124	5.55	0.4325	1.52
1000	un annealed	0.2	7.3	0.12	5.5	0.4520	1.46
	373	0.21	7.35	0.125	5.67	0.4591	1.57
	473	0.215	7.4	0.13	5.75	0.4698	1.64
Illuminated Under Light Power =105mW/cm^2							
t(nm)	**T_a(K)**	**V_{oc}(V)**	**J_{sc} (mA/cm^2)**	**V_{max} (V)**	**J_{max} (mA/cm^2)**	**F.F**	**η %**
400	un annealed	0.3	8.3	0.19	6.9	0.5265	1.24
	373	0.32	8.6	0.21	7.1	0.5417	1.42
	473	0.34	8.8	0.23	7.3	0.5611	1.59
600	un annealed	0.32	8.7	0.21	7.2	0.5431	1.44
	373	0.34	8.9	0.23	7.4	0.5624	1.620
	473	0.36	9.2	0.25	7.6	0.5736	1.809
1000	un annealed	0.36	9.1	0.25	7.5	0.5723	1.78

	373	0.38	9.3	0.26	7.7	0.5664	1.9
	473	0.4	9.4	0.27	8	0.5744	2.05

4. Conclusion

A study on Al/n-CdTe/NiCr Schottky diode structure deposited at273K and annealed at 373K, 473K for different thickness showed that the measured Schottky barrier height increases with the increasing of the thickness and annealing temperatures. The value of barrier height of C-V measurements greater than the value J-V measurements. These are also Short circuit current density (J_{sc}), open circuit voltage (V_{oc}) and efficiency (η **%**) increase with the increasing thickness and annealing temperatures.

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