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Optimisation of Delay and Power Consumption in Fin-FET SRAM Cells

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ABSTRACT

Static Random Access Memory (SRAM) comprises considerable proportion of total area and total power for almost all VLSI chips as cache memory for the System on Chip (SOC) and it is considered to be more intense in upcoming time in both handy devices and high-performance processors. By using low-power FinFET based SRAM cell, we can accomplish higher steadfastness and enhanced battery life for handy devices. Our objective of this work is to improve delay and power consumption in proposed nanoscale 7T FinFET SRAM cell structure. An additional transistor is implemented on FinFET 6T SRAM cell and results are analysed and compared with basic 6T FinFET and proposed 7T FinFET based cell structures on CADENCE VIRTUOSO tool at 45nm technology scale. The power consumption and write delay as well as read delay of proposed 7T FinFET based SRAM cell structure improves with reference to the 6T FinFET SRAM cell architecture.

Keywords: FinFET, Delay, Power consumption, Low power, SRAM cell.

1.INTRODUCTION

In recent decades, VLSI circuit and systems capable of operating reliably at very low voltages became beneficial to portable electronic system having strict power constraints. With lowering of the technology scale, the feature sizes have minimized more and more and tininess at chip level has occurred. Semiconductor memory arrays can be used to store a huge quantity of digital information. The measure of memory quantity is always depends on the application for which it is designed [1]. The persistently growing requirements for enormous memory demands have possessed the fabrication technology and design rules more condensed and impenetrable, it causes larger storage densities per unit information. This trend towards larger storage capacity and superior density will protract to increase in the foremost era of digital system design.

Read/Write memory or random access memory hold instructions for the time being. memory array storage is required for central processing unit to process the function and permit alteration of data bits. The SRAM cell comprises of a latch, it does not require any refresh process, as the cell transistor holds the data as long as the power supply is not disconnect. Large sum of power consumption in handy electronics devices is an concern of serious distress. Supplementary packaging and cooling fans becomes compulsory to minimise the heat dissipation associated with high power consumption, this results in increment of overall chip area [2]. Due to this excessive heat dissipation on the chip, battery life also reduces. Static power dissipation caused due to standby leakage currents, is a vital factor of total power dissipation. Many electronics devices contain different types of component, out of which numerous stay idle during a particular operation. Static power dissipation taking place in these idle components resembles a huge fraction of total power dissipation in the system [2-3]. Therefore, minimization of this leakage factor becomes essential for efficient power management. This paper is organised in order to presents an introductory overview of FinFET and its implementation in SRAM cells, then reviews of the leakage current components inside an SRAM cell and proposed circuit to tackle the issue and finally, the simulation based performance comparison and conclusion derived from this work respectively.

FinFET

FinFET is a piece of equipment which has “fin” similar to the fish, The Source and Drain terminals are like a fin on either side of the Gate and it appears as a “fin”. The Berkeley researchers of California University invented the term FinFET and they confirmed the FinFET as a Non-Planer device.

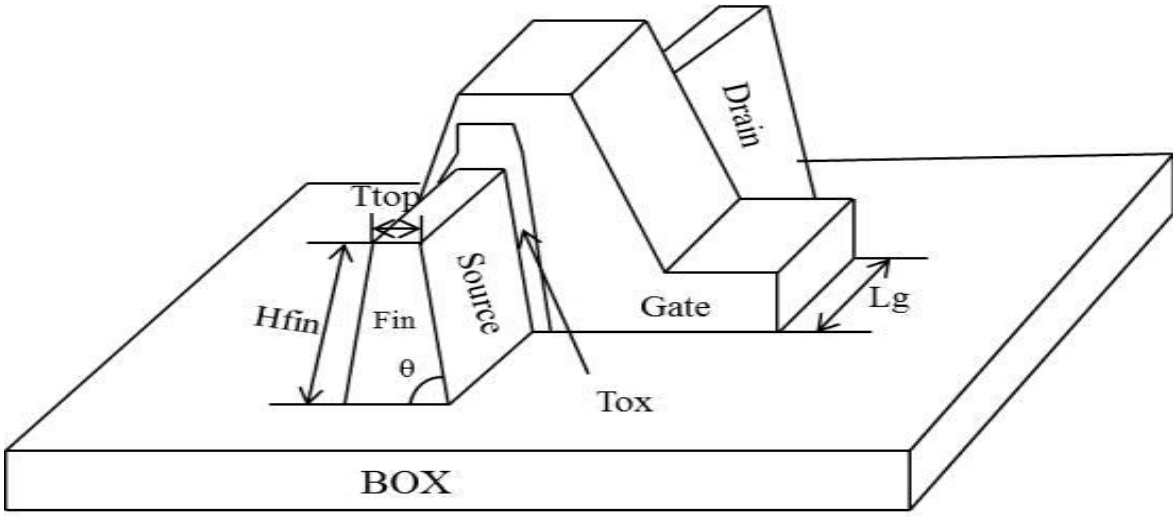

Figure 1: 3D geometry of FinFET

As expressed above, FinFET has structure like "fin" shown in the above figure 1. Here H_{fin} represents the silicon fin's height, L_g represents the FinFET's physical Gate Length, T_{top} represents the silicon fin's thickness and T_{ox} represents the Gate Oxide thickness. If we reduce the channel length more than a specific value then the short channel effect (SCE) come into existence in single gate devices and due to this, the performance of the device starts to degrade. It becomes the most important shortcoming for the devices which have single gate. To overcome this effect, FinFET with Double Gate is introduced which successfully diminish the Short Channel Effect but it requires double power supply for both the Gate, Then the FinFET with Short Gate is introduced which demonstrate immense drop on Short Channel Effect and the problem of double power supply is also removed since both the gates share the same power supply.

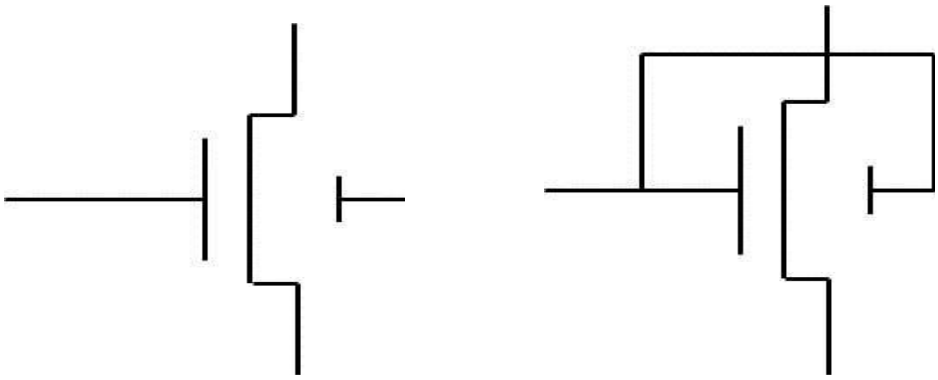

Figure 2: Independent Gate and Short Gate FinFET

FinFET has very excellent Electrostatic control of the channel that is it has full control over channel and boasts a near-ideal sub-threshold performance (associated with leakage), it is not obtained in planer device without extensive effort. FinFET reduces short channel effect to a great extent, which in planer technology are very complex and have a sufficient impact on gate length variation and on electrical performance. FinFET has higher incorporation density and smaller changeability.
FinFET on silicon on insulator is favoured over bulk FinFET [4].Double gate MOSFET and MuGFET are floating body devices into which charge trapping occurs in body this causes leakage due to radiation. Charge trapping occurs due to "back channel interface" and "total dose latch effect" [5]. Trapping in buried oxide potential of body modulates, when depletion between source and body is lesser, then electrons injected into the body and drain region collect it [6].

SRAM Cell
Conventional 6T SRAM cell comprises of two cross coupled inverters M3, M4 and M5, M6 (can be called as latch) and two access transistors M1, M2 shown in Fig 3. Four transistors (M3, M4, M5 and M6) are required to store each bit in an SRAM. The drain terminal of the access transistors (M1 and M2) are connected to the inputs of latch, source terminals are connected to the bit line (BL) and the bit line bar (BLB) [7]. When the word line is low or logic '0', the access transistors are OFF and the bit lines becomes disconnected from latch. In this state, the latch may contain the bit and provided that the voltage remains in V_{DD} and V_{SS}. When the word line is high or logic '1', access transistors are

ON, and bit lines (BL and BLB) becomes connected to the latch, these bit lines are used to convey data for both read and write operations [8-9].

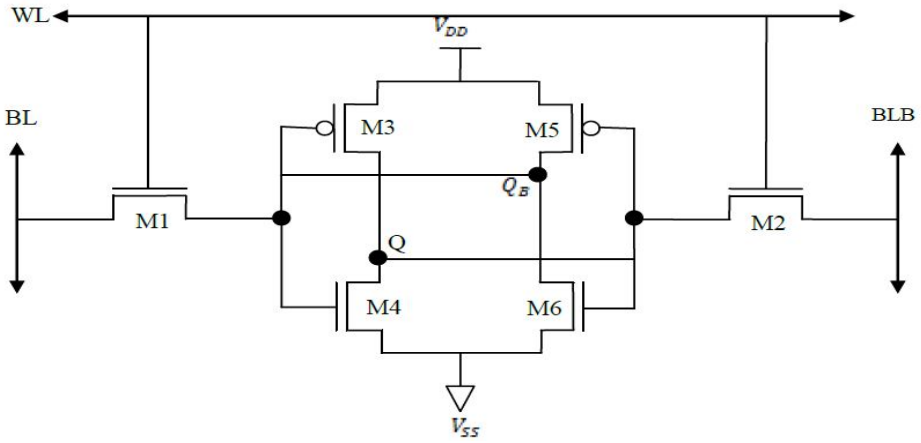

Fig 3: Conventional 6T SRAM Cell

Write Delay

For a write operation, the write delay is defined as the time between the activation 50% of WL to when Qbar is 90% of its full swing [10]. Propagation delay of inv2 and inv l determines the write delay of the cell. Data to be written into the cell is applied to the bit lines (bl and blb). The access transistors are activated by applying the signal voltage to the gates of access transistors or we can say by applying logic "1" to word line WL. When appropriate voltages are applied at bit lines and word line is enabled the node will get the value from the bit line. In write operation for the SRAM cell, a reasonable write-trip point is equally important [10] to guarantee the write ability of the cell without the expenditure of too much power in shifting down the bit-line voltage to 0 V. The write-trip point defines the maximum voltage on the bit-line, essential to flip the cell content. Pull-up ratio of the cell gives the measure of write trip point while the cell ratio of cell gives the measure of read stability.

Leakage Current

When the gate to source voltage Vgs is less than the threshold voltage Vt (Vgs < Vt) then the current that flows from drain to source of the transistor constitutes Sub-threshold leakage [11]. In the sub-threshold region, the drain current depends exponentially on the gate to source voltage and is given by equation (1).

$$I_d \ \alpha \ \exp\left(\frac{Vgs}{Vt}\right) \qquad (1)$$

Where Vt = kT/q

Vt indicates threshold voltage, 'k' indicates the Boltzmann constant, T indicates the absolute temperature, and q indicates the charge of electron. Leakage current is the flow of electrons through the gate that flows when the transistor is in OFF state.

The FinFET based 6T-SRAM cell is designed using FinFET (shorted gate) in place of MOSFETs in conventional 6T-SRAM cell; it is shown in fig.4 below.

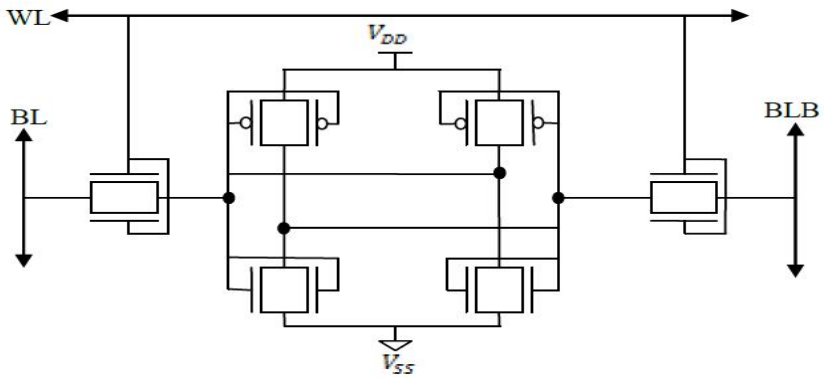

Fig 4 FinFET based 6T SRAM cell

Now the proposed FinFET based 7T SRAM cell structure shown in Fig.5. This cell consists of an additional FinFET placed in the cell's ground path to reduce leakage while the cell is in hold mode. In hold mode, the extra transistor which is placed at bottom is projected to cut-off the ground path and eliminates the paths through which the leakage can occur in the inverter of the cell. The gate of bottom FinFET is connected to the word line. The bottom FinFET is indistinguishable in size to the inverter FinFET to match their current carrying capacity.

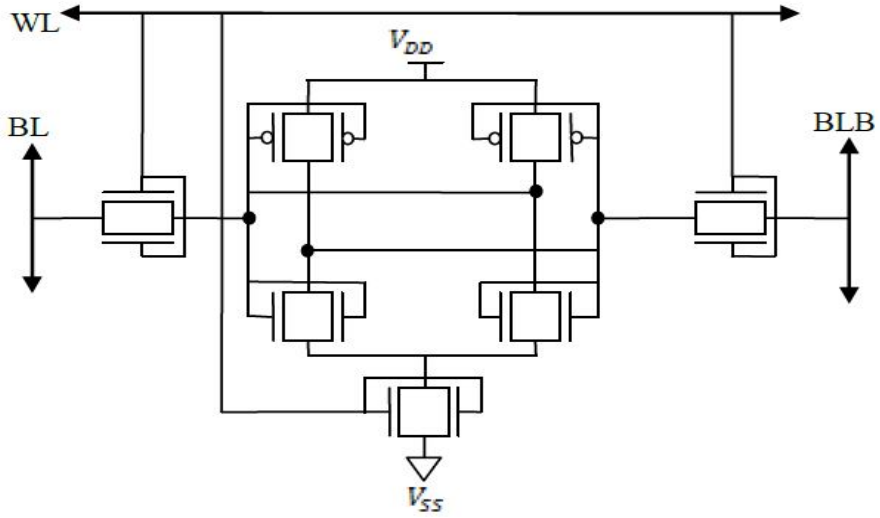

Fig 5 FinFET based proposed 7T SRAM cell

2.SIMULATION RESULTS

The architecture of FinFET 6T SRAM cell is customized by using an extra transistor in ground path. The circuit designed using the Analog Cadence Virtuoso; all waveforms are plotted in Cadence SPECTRE simulator. We obviously see that proposed 7T SRAM cell shows a excellent performance in terms of leakage power, leakage current, write delay and read delay of the cell compared with FinFET 6T SRAM cell. . In the modified architecture, the threshold voltages, W/L ratios of all the transistors and the power supply were same as of the parent architectures and one transistor is inserted at the bottom of the SRAM cell in the proposed technique. The analysed parameters of FinFET 6T cell and proposed FinFET 7T cell are shown in waveforms below.

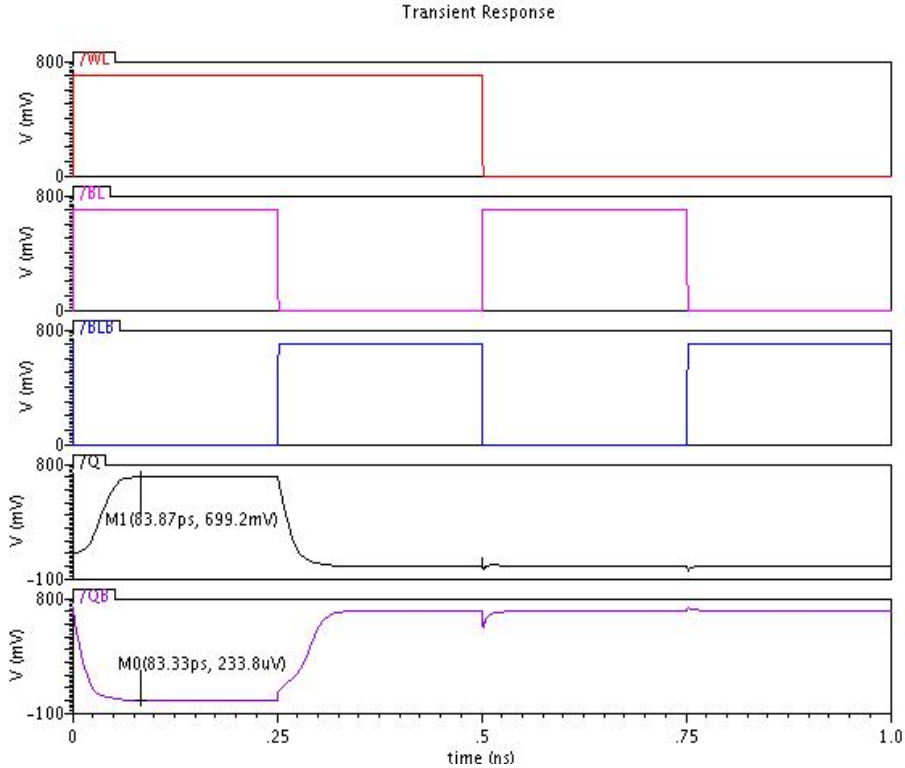

Fig 6: The waveform of write operation in FinFET based 6T SRAM cell.

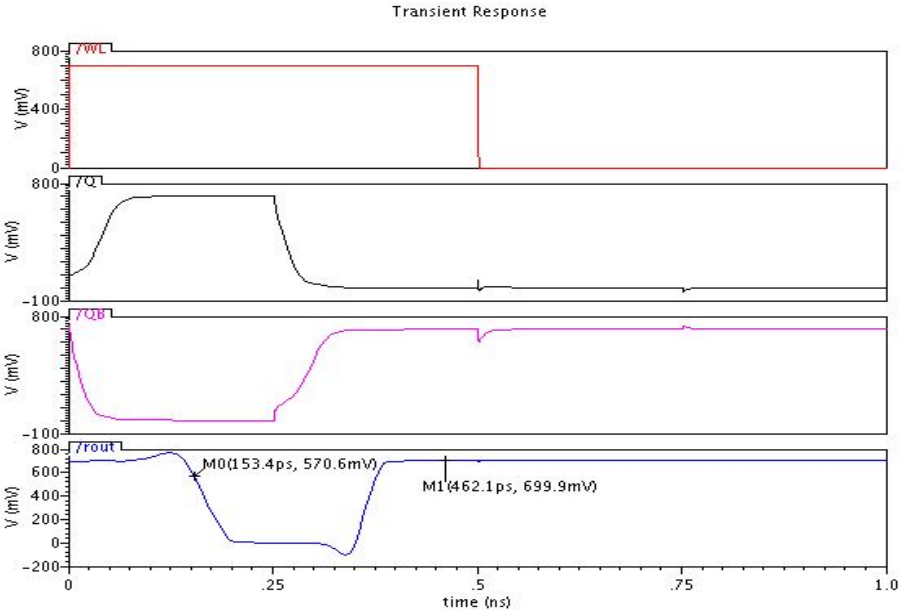

Fig 7: The waveform of read operation in FinFET based 6T SRAM cell.

Above Fig.6, 7 is showing the waveform for the writing and the reading operation according to the FinFET 6T SRAM cell. In the waveform BL and BLB refers bit and bit line bar, respectively. The voltage level on all sources was maintained at 700 mV. In Fig 6a, when the word line is high or logic '1' the Q and Q_b output change the states according to BL and BLB, when WL goes low or logic '0' SRAM holds the data.

Fig 8 and 9 below shows the waveform of the total leakage power and the total leakage current in FinFET based 6T SRAM cells. The total leakage power and total leakage current are 10.73nW and 78.59fA respectively.

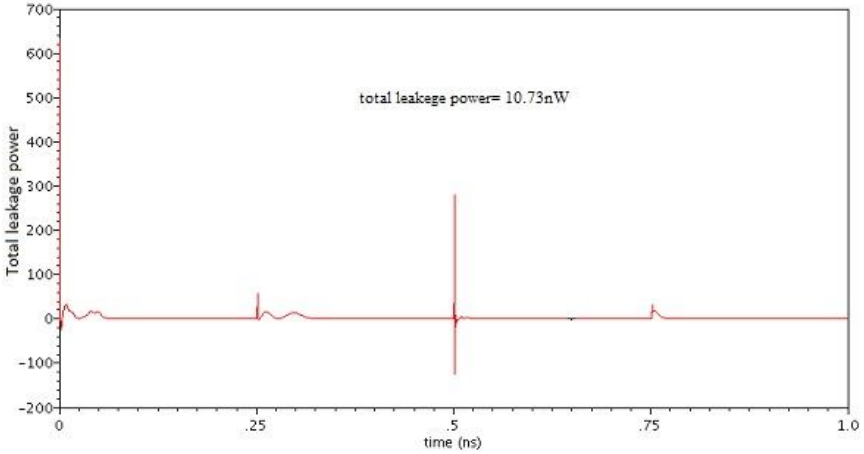

Fig 8: The waveform of total leakage power in 6T FinFET SRAM cell.

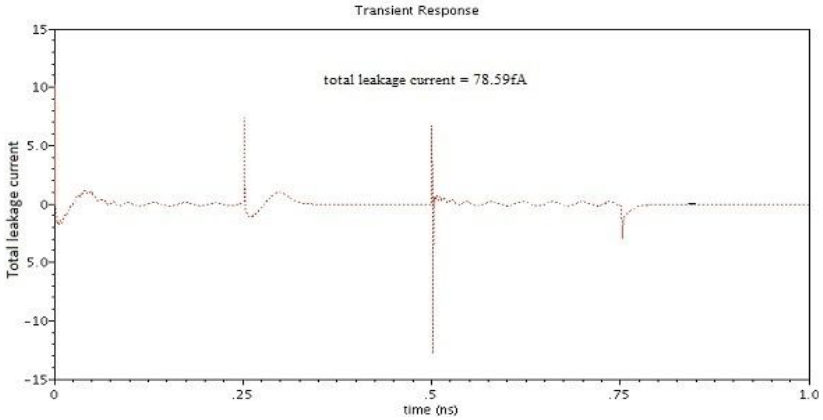

Fig 9: The waveform of total leakage current in FinFET based 6T SRAM cell.

Fig 10 and 11 below shows the waveform for the writing and reading operation of the proposed FinFET 7T SRAM cell. In the waveform BL and BLB refers to bit line and bit line bar, respectively. The voltage level on all sources was kept at 700 mV.

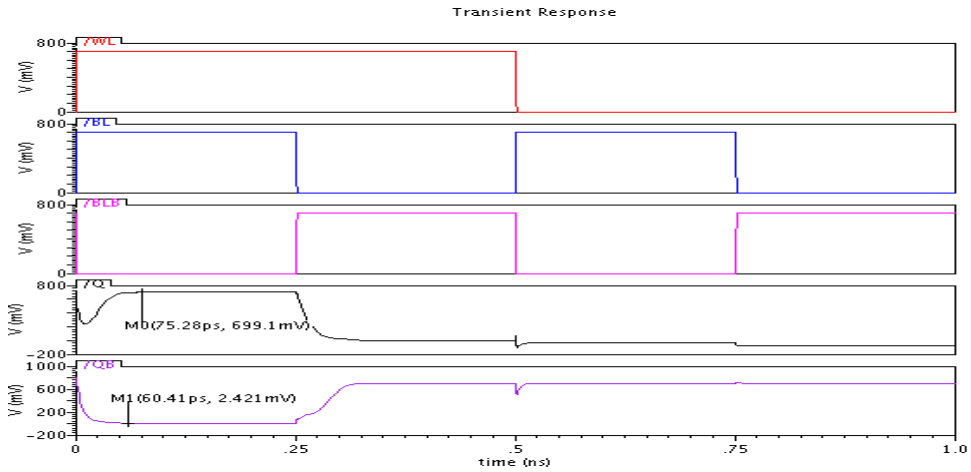

Fig 10: The waveform of write operation in FinFET based 7T SRAM cell.

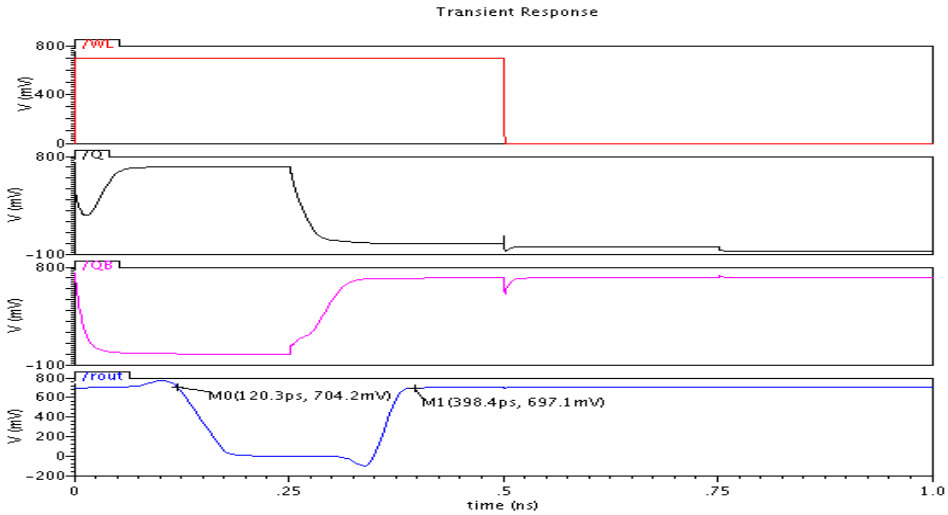

Fig 11: The waveform of read operation in FinFET based 7T SRAM cell.

Fig 12 and 13 below shows the waveform for the total leakage current and the total leakage power in FinFET based 7T SRAM cell. The total leakage current and total leakage power are 57.37fA and 7.19nW respectively.

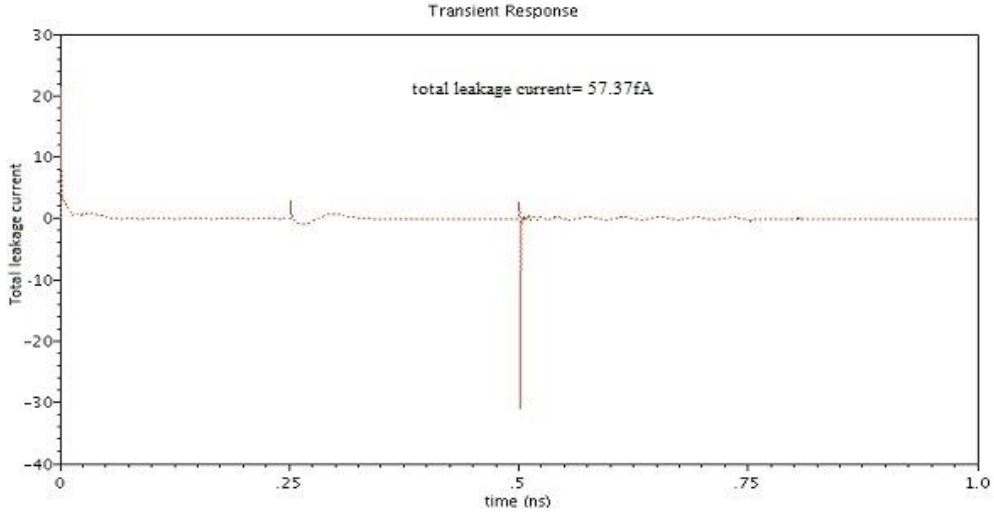

Fig 12: The waveform of total leakage current in FinFET based 7T SRAM cell.

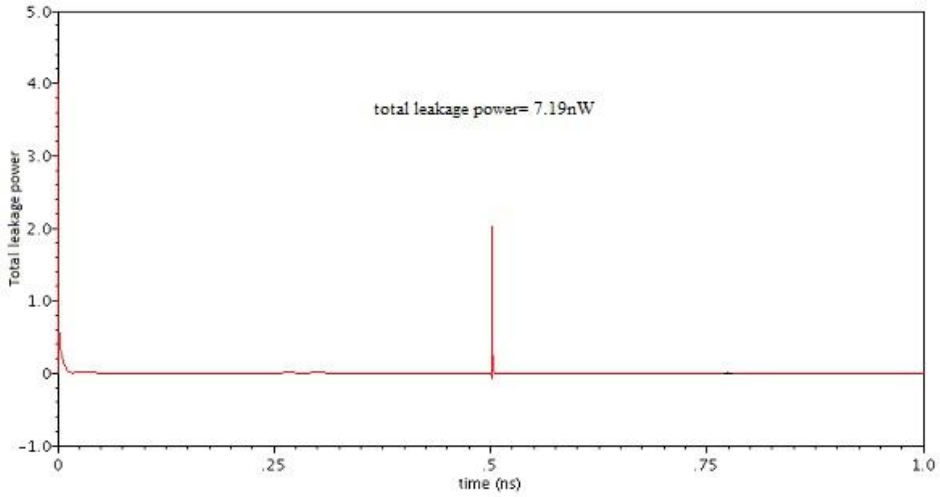

Fig 13: The waveform of total leakage power in FinFET based 7T SRAM cell.

The results obtained from the cadence virtuoso simulator are summarized in Table I. In Table I, Twrite0 and Twrite1 are called writing time of bit '0' and bit '1' and then Tread0 and Tread1 are called as reading time of bit '0' and bit '1' respectively. It is observed that the writing time of FinFET based 7T SRAM for the bit '0' and '1' are less as compared to the FinFET based 6T SRAM cell, and reading time of FinFET based 7T SRAM for bit '0' and '1' are also less as compared to the FinFET based 6T SRAM cell.

Table 1 Simulation results of FinFET based 6T SRAM cell and proposed 7T SRAM cell.

Parameters	**6T FinFET SRAM cell**	**Proposed 7T FinFET SRAM cell**
Technology	45nm	45nm
Supply	700mV	700mV
Leakage current	78.59fA	57.37fA
Leakage power	10.73nW	7.19nW
T_{read0}	153.4ps	120.3ps
T_{read1}	462.1ps	398.4ps
T_{write0}	83.33ps	60.41ps
T_{write1}	83.87ps	75.28ps

3.CONCLUSION

Analysis of numerous parameters of the FinFET based 6T and proposed 7T SRAM cells described here in as leakage current, leakage power, read speed and write speed. The analysis of all parameters was performed using the Analog Cadence Virtuoso tool. The proposed FinFET based 7T SRAM cell is the faster cell to perform read and write operation and gave much better performance to leakage power and leakage current as compared to FinFET based 6T SRAM cell. The present work analyzes the latest developments in low-power circuit techniques and methods with an emphasis on FinFET SRAMs. Appropriate approach for improvement of power consumption and speed were studied such as capacitance reduction, very low operating voltages, DC and AC current reduction and suppression of leakage currents to name a few. The proposed circuit is topology based and hence easier to implement. The substantial reduction in leakage currents (27%), leakage power (33%) and delay obtained, proves them to be very effective as far as any fabrication level technique is concerned.

4.Acknowledgement

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