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An Analysis of Noble 12T SRAM cell with different performance parameter at 32 NM Technology

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ABSTRACT

Leakage power dissipation, read delay, write delay and I_{ON}/I_{OFF} are initial parameters which are practically positive in low power applications. Now a day's low power applications are valuable in semiconductor devices. This paper presents a noble 12T SRAM cell where we use Schmitt trigger circuit and conventional transistor to augment cell performance. Firstly we analysis proposed 12T SRAM cell with conventional 6T, 9T, 10T and 11T SRAM cell in different parameters and compares them in 0.9 volt at 32nm technology. Results are enhanced inread delay, I_{ON}/I_{OFF}, leakage current and power dissipation.

Keywords -Leakage power, Read delay, $I_{ON}/I_{OFF,}$ Schmitt trigger

1. INTRODUCTION

Now a day, there is a high necessitate of multi-operation system which available in one device like portable electronic devices[1].A portable electronic device requires low power and high stability[2]. Low power is a main consent for device performance.Therefore, in this paper we analyzing various parameter according toadd to cell performance in low power.In conventional 6T SRAM Cellperformance is limited byundesirable time taken by access transistors for make active both inverters with high power supply[3].

As nanometer scaling increases leakage current variations and power dissipation also increases. High leakage current can create problem of power consumption. For nanotechnologyintegrated circuits support complex designs. These complex designs form for high speed and low power consumption but leakage current decrease the performance of circuit by increasing power dissipation.

Read delay and Write delay is define time delay in sensing the data in output[4].The accessibility of the cell is depend on read / write delay.Differential SRAMcell shows less delay compare to single ended SRAM cell[4] which is a key aspect of proposed SRAM cell regarding delay factor.

This work present a novel 12T SRAM Cell in 32 nm Technology at 0.9 volt. In this paper we show the comparison of proposed SRAM cell with other SRAM cell and vary them in various parameters for analyses in low power variation. The leakage, power dissipation, read/write delay and I_{ON}/I_{OFF} ratio are discussed in read, write and hold operation.

This paper is making as follows. An overview of the literature review is presented in Section II. Experimental resultshas been discussed in Section III where read delay, write delay, I_{ON}/I_{OFF} , leakage and power dissipation parameter has been compared with proposed cell. Section IVhas conclusion where we summers overview of all results.

2. Literature Review

This article presents the simulation of 6T, 9T, 10T, 11T and proposed 12T SRAM cell. All the simulations have been happened at spice tool.

2.1 Conventional 6T SRAM cell

The conventional 6T SRAM cell construct by two inverter latches which is cross coupled with two access transistors connected to a complimentary bit lines as shown in Figure 1. The access transistors are attached to theword Line (WL), where WL is high for read and write operation. The bit line and bit line bar act as Input/output buses which take the data from the SRAM cell to the sense amplifier [5]shown in Figure1.

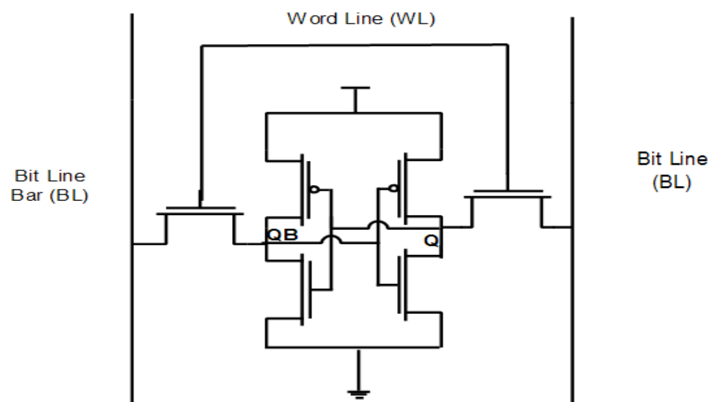

Figure.1 Conventional 6T SRAM cell

2.2 9T SRAM Cell

The 9T SRAM cell [6] is shown in Figure 2. Write and read operation occur separately.Write operation in 9T SRAM cell occurs similar to 6T SRAM cell. Reading operation occurs when read signal (RWL) going high. This 9T SRAM cell has a drawback of high bit line capacitance with extra pass transistors on the bit line of SRAM cell.

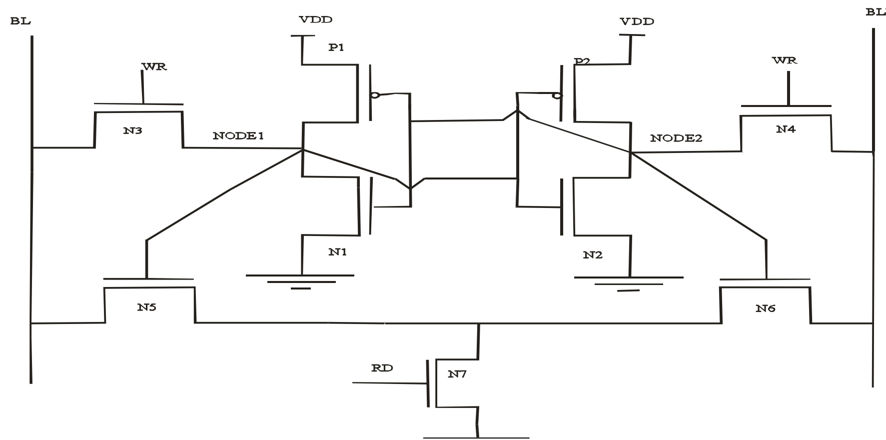

Figure2. 9T SRAM cell

2.3 10T SRAM cell

The 10T SRAM cell [7] is shown in Fig. 3. The design strategy of cell is based on 6T SRAM cell, where N5 and N8 are used to isolate Q/QB nodes from bit lines in the read operation. In write /read operation separate word lines a also used in this SRAM design (WWL and RWL). Here this design uses storage structure like 6TSRAM cell.10T SRAM cell ensure thatQ and QB nodes are not affected by pre-charged values which is stored in BL and BLB during read operation.

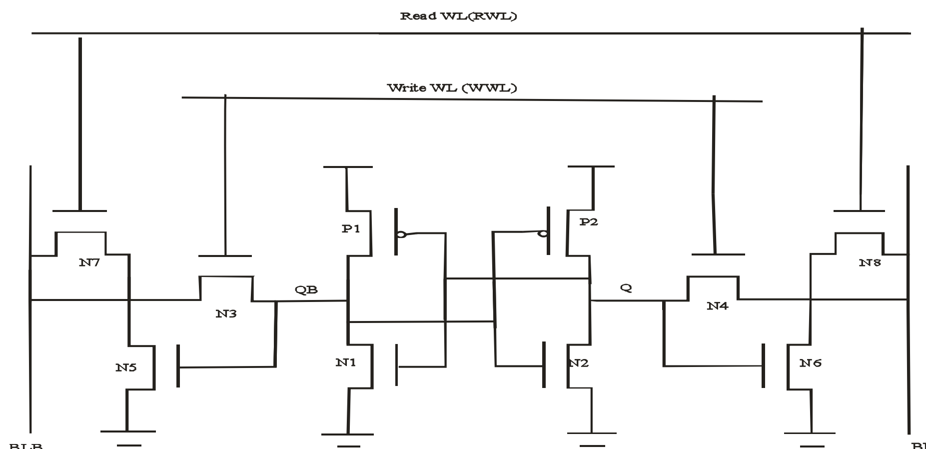

Figure3.10T SRAM cell

2.4 11T SRAM cell

The 11T SRAM cell [8] is shown in Fig.4.Here this design using single ended SRAM cell designwith Schmitt-Trigger to robust SRAM cell. Single-ended SRAM design is exceedingly useful for low power applications. Schmitttriggers are used toenhance the inverter characteristic in this design where conventional 6T SRAM cell has drawback of it.

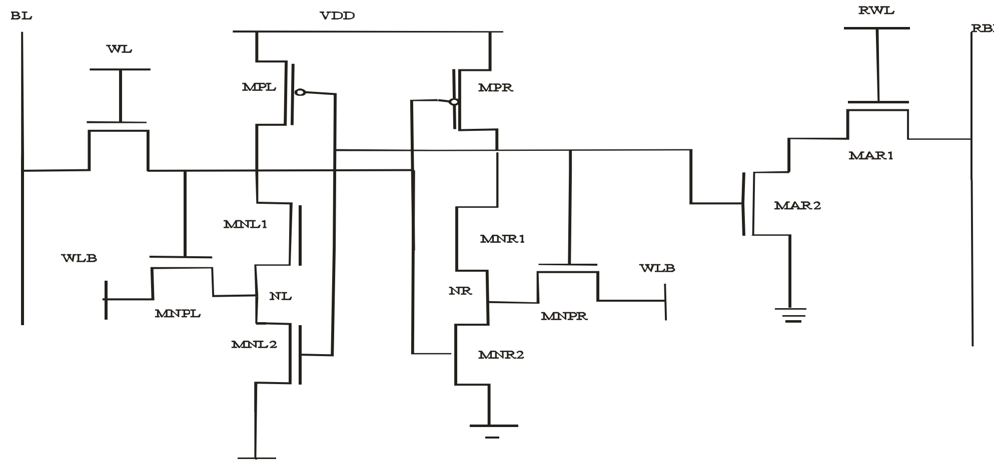

Figure4. 11T SRAM cell

2.5 Proposed 12T SRAM cell

The proposed cell has been constructing with the help of schmitt trigger and a conventional transistor shown inFigure5. Schmitt trigger is used to give positive feedback and conventional transistor is used to decrease leakage current compare to other SRAM cell structures. The read, write and hold operation simulation result has been discussed.

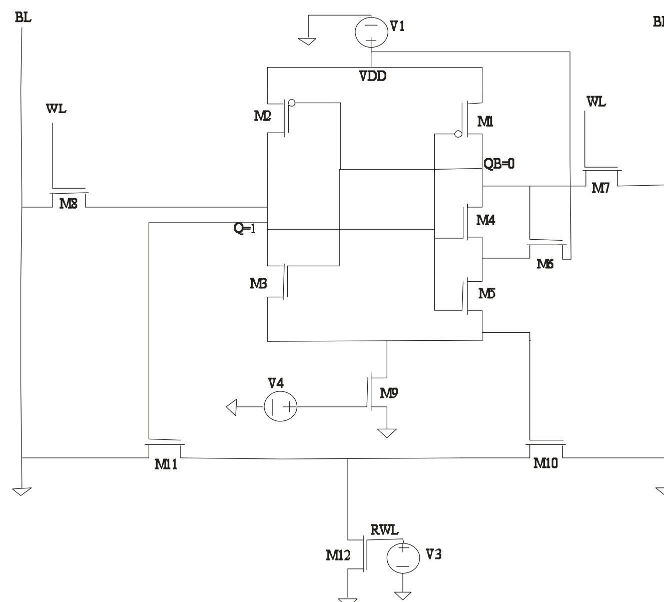

Figure5. Proposed 12T SRAM cell

3. Experimental results

In this section, read delay, write delay, I_{ON}/I_{OFF}, leakage and power dissipation for SRAM cells has been discussed.All parameter are measured in low power supply. All results are measured in spice simulator at 32 nm technology.Figure 6 shows the Write, Read and Hold waveforms for proposed 12T SRAM cell[9]. Figure 7 show the simulation results of Conventional 6T, 9T, 10T, 11T and proposed 12T SRAM cell in Read Delay parameter[3]. Similarly simulation results of Conventional 6T,9T,10T,11T and proposed 12T SRAM cell in write delay, leakage, power dissipation and $I_{ON}/I_{OFF}$are show in respectively.Comparative table of Read Delay,Write Delay,I_{ON}/I_{OFF} Ratio,Leakage power and variation in supply vage are shown in Table1and Table2 respectively.

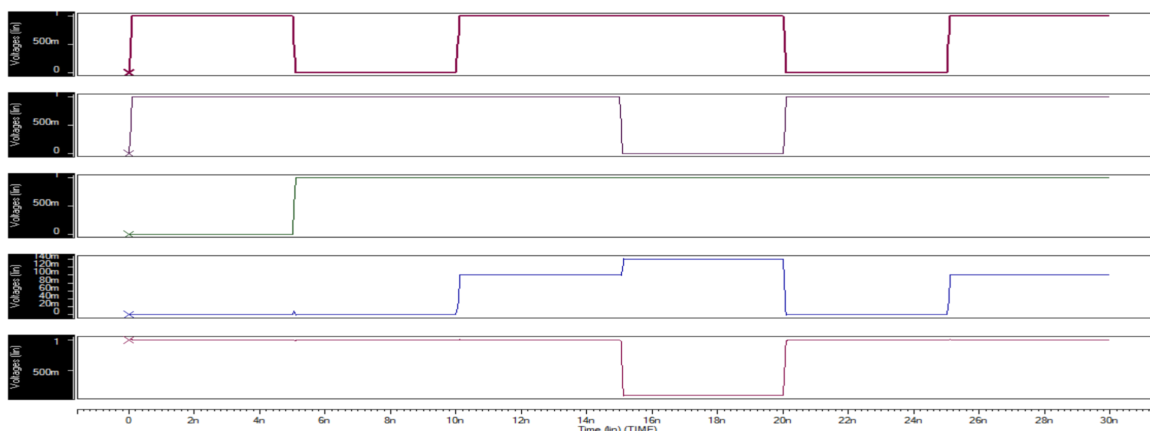

Figure6. Write, Read and Hold waveforms of proposed 12T SRAM cell

3.1 Read Delay

Read delay is the delay concerned in allowing the bit lines to discharge nearly 10% of the highest value or the delay between the function of the WL signal and the response time of the sense amplifier[10]. Read delay of proposed 12T SRAM cell is minimum compare to 9T, 10T, 11T SRAM cell but little bit higher compare to 6t SRAM cell.

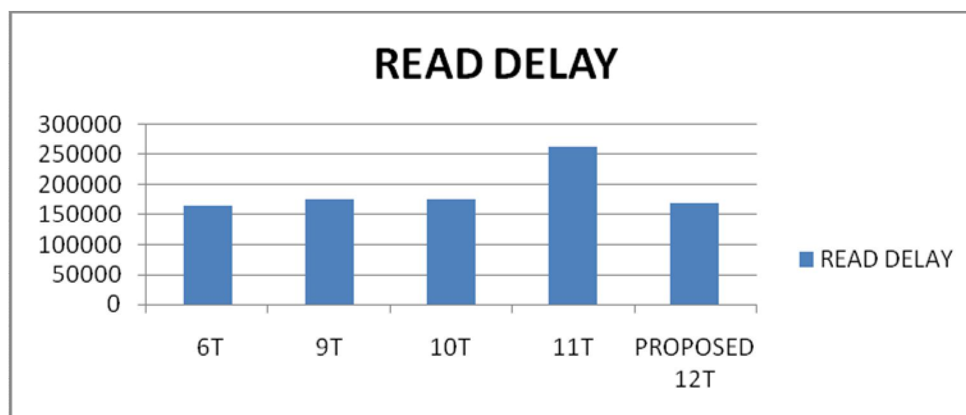

Figure7. Comparative value of Read Delay of SRAM cell

3.2 Write Delay

It is the delay between thefunctions of the word line WL signal and the time at which the data is really written in the SRAM cell [10]shown in Figure8. Proposed 12T SRAM cell is lower compare to 11T SRAM cell but higher compare to 6T, 9Tand 10T SRAM cell.

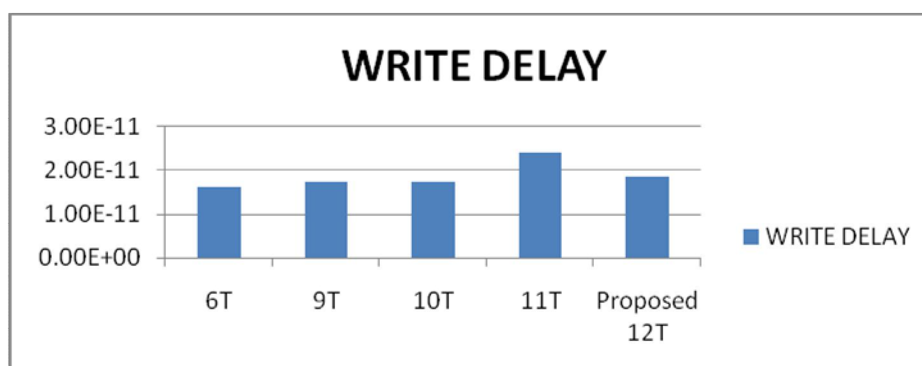

Figure8. Comparative of valueWrite Delay of SRAM cell

3.3 Leakage Current

Leakage current is the current which is leak through transistors. The main contributor of leakage is the sub-threshold leakage current. It requires low electric field and large power supply. Practically leakage current simulated during hold operation[11]shown in Figure9. Here proposed 12T SRAM cell showing minimum leakage current compare to 6T, 10T, 11T SRAM cell and equal to 9T SRAM cell.

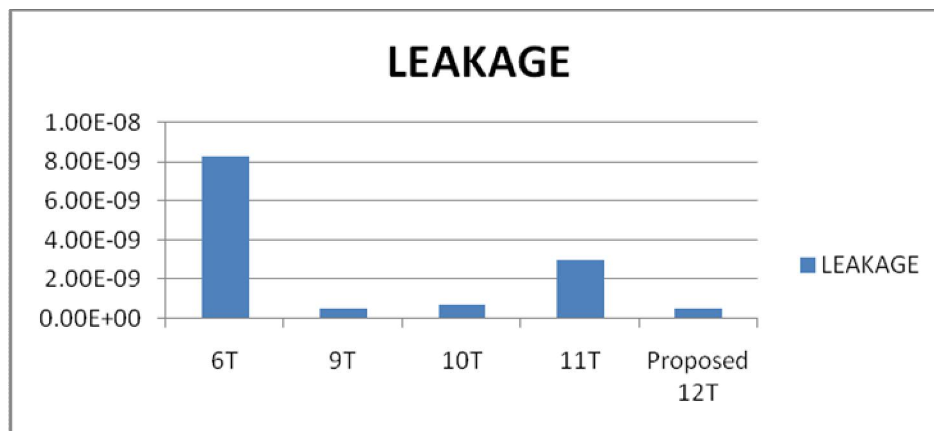

Figure9. Comparative value ofLeakage Current of SRAM cell

3.4 Power Dissipation

Power dissipation is a combination of static and dynamic power dissipation. Static power dissipation is a main factor of the total power. Static power is occurring in a cell design in the absence of any switching activity and is defined as the product of supply voltage and leakage current[12]shown in Figure10. Here proposed 12T SRAM cell showing minimum power dissipation compare to 6T, 9T, 11T SRAM cell and higher compare to 10T SRAM cell.

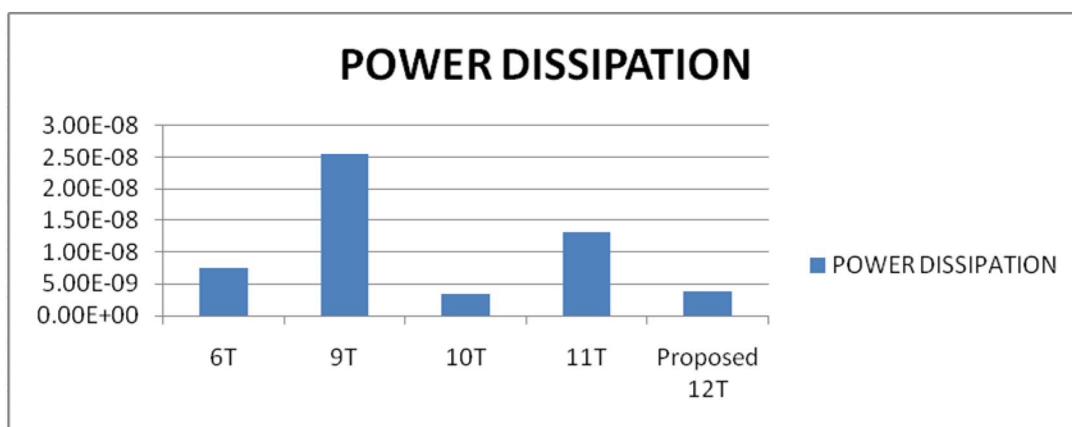

Figure10. Comparative value of Power Dissipation of SRAM cell

3.5 I_{ON}/I_{OFF}Ratio

I_{ON} current defines drain current of access transistor and I_{OFF}currentshowing leakage current in SRAM cell design. So, I_{ON}/I_{OFF}ratioshows the accessibility of nmos and pmos transistorshown in Figure11.Here, proposed 12T SRAM cell showing higher I_{ON}/I_{OFF}ratio compare to 6T and 11T SRAM cell and equal to 9T and 10T SRAM cell.

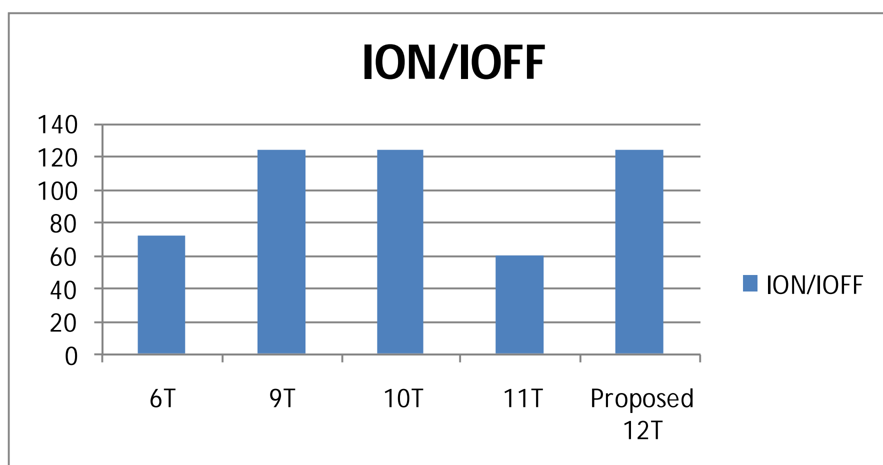

Figure11. Comparative value of I_{ON}/I_{OFF} Ratio of SRAM cell

Table1. Comparative table of Read Delay,Write Delay,I_{ON}/I_{OFF} Ratio,Leakage power of SRAM cell

CELL / PARAMETER	Conventional 6T SRAM cell	9T SRAM cell[6]	10T SRAM cell [7]	11T SRAM cell [8]	Proposed 12T SRAM cell
Read Delay	2.6689E-12	2.8724E-12	2.8548E-12	1.5818E-11	2.7626E-12
Write Delay	4.7525E-11	5.0673E-11	5.1917E-11	2.41E-11	8.5309E-11
I_{ON}/I_{OFF} Ratio	71.81628721	123.7701687	123.7701687	0.3572313089	123.7701687
Leakage power	8.3153 E-09	545.3815E-12	732.2365E-12	13.0948E-09	545.3629E-12

Table2. Comparative table ofSupply Voltage of SRAM cell

CELL / SUPPLY VOLTAGE	Conventional 6T SRAM cell	9T SRAM cell[6]	10T SRAM cell[7]	11T SRAM cell[8]	Proposed 12T SRAM cell
1	2.1465E-12	2.3090E-12	2.2929E-12	6.9888E-12	2.2287E-12
0.9	2.6689E-12	2.8724E-12	2.8548E-12	1.5818E-11	2.7626E-12
0.8	3.5256E-12	3.8097E-12	3.7919E-12	6.0209E-11	3.6587E-12
0.7	5.2425E-12	5.6801E-12	5.6663E-12	1.3605E-10	5.4875E-12
0.6	9.8536E-12	1.0659E-11	1.0622E-11	-	1.0554E-11
0.5	2.5621E-11	2.8507E-11	3.1048E-11	-	3.0659E-11
0.4	1.1402E-10	1.4266E-10	-	-	1.0167E-10

4. Conclusion

A proposed 12T SRAM cell which have schmitttriggerand a conventional transistor achieve low leakage current. Simulate result with 6T, 9T, 10T and 11T SRAM cell with spice simulator. The proposed 12T SRAM cellenhanced read delay, I_{ON}/I_{OFF}, leakage current and powerdissipation compare to 6T, 9T,10T,11T at 0.9 volt.Also proposed SRAM cell achieve low write delay compare to 11T SRAM cell.Simulation and analysing performance of Proposed SRAM cell at 32nm technology.

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