An Analysis of Noble 12T SRAM cell with different performance parameter at 32 NM Technology

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ABSTRACT

Leakage power dissipation, read delay, write delay and ION/IOFF are initial parameters which are practically positive in low power applications. Now a day’s low power applications are valuable in semiconductor devices. This paper presents a noble 12T SRAM cell where we use Schmitt trigger circuit and conventional transistor to augment cell performance. Firstly we analysis proposed 12T SRAM cell with conventional 6T, 9T, 10T and 11T SRAM cell in different parameters and compares them in 0.9 volt at 32nm technology. Results are enhanced in read delay, ION/IOFF, leakage current and power dissipation.

Keywords -Leakage power, Read delay, ION/IOFF, Schmitt trigger

1. INTRODUCTION

Now a day, there is a high necessitate of multi-operation system which available in one device like portable electronic devices[1]. A portable electronic device requires low power and high stability[2]. Low power is a main consent for device performance. Therefore, in this paper we analyzing various parameter according to cell performance in low power. In conventional 6T SRAM Cell performance is limited by undesirable time taken by access transistors for make active both inverters with high power supply[3].

As nanometer scaling increases leakage current variations and power dissipation also increases. High leakage current can create problem of power consumption. For nanotechnology integrated circuits support complex designs. These complex designs form for high speed and low power consumption but leakage current decrease the performance of circuit by increasing power dissipation.

Read delay andWrite delay is define time delay in sensing the data in output[4]. The accessibility of the cell is depend on read / write delay. Differential SRAM cell shows less delay compare to single ended SRAM cell[4] which is a key aspect of proposed SRAM cell regarding delay factor.

This work presents a novel 12T SRAM Cell in 32 nm Technology at 0.9 volt. In this paper we show the comparison of proposed SRAM cell with other SRAM cell and vary them in various parameters for analyses in low power variation. The leakage, power dissipation, read/write delay and ION/IOFF ratio are discussed in read, write and hold operation.

This paper is making as follows. An overview of the literature review is presented in Section II. Experimental resultshas been discussed in Section III where read delay, write delay, ION/IOFF, leakage and power dissipation parameter has been compared with proposed cell. Section IV has conclusion where we summers over view of all results.

2. Literature Review

This article presents the simulation of 6T, 9T, 10T, 11T and proposed 12T SRAM cell. All the simulations have been happened at spice tool.

2.1 Conventional 6T SRAM cell

The conventional 6T SRAM cell construct by two inverter latches which is cross coupled with two access transistors connected to a complimentary bit lines as shown in Figure 1. The access transistors are attached to the word Line (WL), where WL is high for read and write operation. The bit line and bit line bar act as Input/output buses which take the data from the SRAM cell to the sense amplifier [5] shown in Figure 1.
2.2 9T SRAM Cell
The 9T SRAM cell [6] is shown in Figure 2. Write and read operation occur separately. Write operation in 9T SRAM cell occurs similar to 6T SRAM cell. Reading operation occurs when read signal (RWL) going high. This 9T SRAM cell has a drawback of high bit line capacitance with extra pass transistors on the bit line of SRAM cell.

2.3 10T SRAM cell
The 10T SRAM cell [7] is shown in Fig. 3. The design strategy of cell is based on 6T SRAM cell, where N5 and N8 are used to isolate Q/QB nodes from bit lines in the read operation. In write/read operation separate word lines are also used in this SRAM design (WWL and RWL). Here this design uses storage structure like 6T SRAM cell. 10T SRAM cell ensure that Q and QB nodes are not affected by pre-charged values which is stored in BL and BLB during read operation.
2.4 11T SRAM cell
The 11T SRAM cell [8] is shown in Fig. 4. Here this design using single ended SRAM cell design with Schmitt-Trigger to robust SRAM cell. Single-ended SRAM design is exceedingly useful for low power applications. Schmitt triggers are used to enhance the inverter characteristic in this design where conventional 6T SRAM cell has drawback of it.

![Figure 4. 11T SRAM cell](image)

2.5 Proposed 12T SRAM cell
The proposed cell has been constructing with the help of schmitt trigger and a conventional transistor shown in Figure 5. Schmitt trigger is used to give positive feedback and conventional transistor is used to decrease leakage current compare to other SRAM cell structures. The read, write and hold operation simulation result has been discussed.

![Figure 5. Proposed 12T SRAM cell](image)

3. Experimental results
In this section, read delay, write delay, I\text{ON}/I\text{OFF}, leakage and power dissipation for SRAM cells has been discussed. All parameter are measured in low power supply. All results are measured in spice simulator at 32 nm technology. Figure 6 shows the Write, Read and Hold waveforms for proposed 12T SRAM cell[9]. Figure 7 show the simulation results of Conventional 6T, 9T, 10T, 11T and proposed 12T SRAM cell in Read Delay parameter[3]. Similarly simulation results of Conventional 6T,9T,10T,11T and proposed 12T SRAM cell in write delay, leakage, power dissipation and I\text{ON}/I\text{OFF} are show in respectively. Comparative table of Read Delay, Write Delay, I\text{ON}/I\text{OFF} Ratio, Leakage power and variation in supply vage are shown in Table 1 and Table 2 respectively.
3.1 Read Delay
Read delay is the delay concerned in allowing the bit lines to discharge nearly 10% of the highest value or the delay between the function of the WL signal and the response time of the sense amplifier[10]. Read delay of proposed 12T SRAM cell is minimum compare to 9T, 10T, 11T SRAM cell but little bit higher compare to 6T SRAM cell.

3.2 Write Delay
It is the delay between the functions of the word line WL signal and the time at which the data is really written in the SRAM cell [10] shown in Figure 8. Proposed 12T SRAM cell is lower compare to 11T SRAM cell but higher compare to 6T, 9T and 10T SRAM cell.

3.3 Leakage Current
Leakage current is the current which is leak through transistors. The main contributor of leakage is the sub-threshold leakage current. It requires low electric field and large power supply. Practically leakage current simulated during hold operation[11] shown in Figure 9. Here proposed 12T SRAM cell showing minimum leakage current compare to 6T, 10T, 11T SRAM cell and equal to 9T SRAM cell.
3.4 Power Dissipation
Power dissipation is a combination of static and dynamic power dissipation. Static power dissipation is a main factor of the total power. Static power is occurring in a cell design in the absence of any switching activity and is defined as the product of supply voltage and leakage current[12] shown in Figure10. Here proposed 12T SRAM cell showing minimum power dissipation compare to 6T, 9T, 11T SRAM cell and higher compare to 10T SRAM cell.

3.5 I_{on}/I_{off} Ratio
I_{on} current defines drain current of access transistor and I_{off} current showing leakage current in SRAM cell design. So, I_{on}/I_{off} ratio shows the accessibility of nmos and pmos transistor shown in Figure11. Here, proposed 12T SRAM cell showing higher I_{on}/I_{off} ratio compare to 6T and 11T SRAM cell and equal to 9T and 10T SRAM cell.
Table 1. Comparative table of Read Delay, Write Delay, $I_{ON}/I_{OFF}$ Ratio, Leakage power of SRAM cell

<table>
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<tbody>
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<td>Read Delay</td>
<td>2.6689E-12</td>
<td>2.8724E-12</td>
<td>2.8548E-12</td>
<td>1.5818E-11</td>
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<td>$I_{ON}/I_{OFF}$</td>
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<td>732.2365E-12</td>
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<td>545.3629E-12</td>
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Table 2. Comparative table of Supply Voltage of SRAM cell

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<td>-</td>
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4. Conclusion

A proposed 12T SRAM cell which have schmitt trigger and a conventional transistor achieve low leakage current. Simulation result with 6T, 9T, 10T and 11T SRAM cell with spice simulator. The proposed 12T SRAM cellenhanced read delay, $I_{ON}/I_{OFF}$, leakage current and powerdissipation compare to 6T, 9T, 10T, 11T at 0.9 volt. Also proposed SRAM cell achieve low write delay compare to 11T SRAM cell. Simulation and analysing performance of Proposed SRAM cell at 32nm technology.

References


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