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Comparison of Noise, Power and Delay of Different Multiplier's using Variable Threshold MOSFET in 45nm Technology

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ABSTRACT

In the modern time designing a circuit that consumes less power with minimum delay and noise is one of the major challenges. Normally the circuits are design in CMOS technology. But we know Dynamic Threshold MOSFET (DTMOS) consumes less power than CMOS as it is operated in sub-threshold region and the leakage current is used for its computational operation. Now to reduce the power consumption further and achieve an ultra-low power region of operation Variable Threshold MOSFET (VTMOS) is introduced. In this paper we design a Baugh Woley, Braun and Vedic Multiplier using VTMOS calculated its noise, power and delay in T-spice and a comparison of those circuits with the conventional CMOS design has been done. The circuits have also been implemented by Xilinx 10.1.

Key-Words: VTMOS, Braun Multiplier, Baugh Wooley Multiplier, Vedic Multiplier.

1. INTRODUCTION

In the modern era, operating a MOSFET in low power region is the prime objective of the research field. This advantage of low power MOSFET is especially attractive for developing medical devices like (Hearing aids, pacemakers etc.), sensors and devices [1]. If the transistor below its threshold voltage the power consumption will automatically reduce. To implement this concept DTMOS is introduced, where the MOSFET is to operate in the sub-threshold region and the leakage current is used as computational current in circuits. Now if we give a proper bias voltage applied between gate and substrate, it leads to lowering operating currents and power dissipation. This arrangement is called as VTMOS. VTMOS is nothing but an extension of DTMOS in the sense that the substrate voltage always differs by a fix voltage from the gate voltage. As shown in Fig 1, by connecting positive bias between gate and substrate for NMOS and negative bias between gate and substrate for PMOS, there is rapid reduction of power dissipation in VTMOS when compared to DTMOS and traditional CMOS. The circuit is named as VTMOS because, we have used the same DTMOS with a biased voltage between gate and substrate .The voltage of each transistor is dynamically adjusted depending on gate voltage, causing the threshold voltage of device to adjust dynamically. In this paper, we have designed and implement the VTMOS for designing the different Multiplier's like Baugh Wooley, Braun Multiplier and Vedic Multiplier and simulate and power, delay measure of the circuit in T-spice and compare and analyze the result with conventional approach and show the usefulness of VTMOS in term of power consumption and delay and noise.

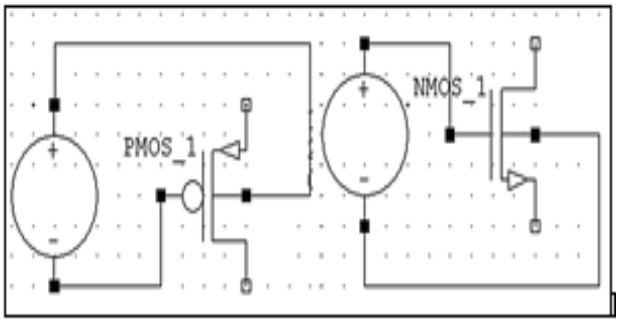

Fig.1. Structure of VTPMOS and VTNMOS

2. PROBLEM FORMULATION

2.1 Current- Voltage Characteristic

For evaluating the I-V characteristics of NMOS devices under VTMOS operating condition, the I-V characteristics are measured and are given in Fig.2, To examine the effects of substrate bias on I-V output characteristics of NMOS under VTMOS operating condition, drain current Ids for different Vds voltages varying from 0 to 150mV and the output is shown in Fig 2.It may be seen that the variation in Ids with drain voltage,Vds becomes less as VIN is made positive (deep sub- threshold region).The input characteristic is also shown in Fig.3. Here, the conducting channel acts as a resistance and because of that the drain current ID is proportional to the drain-source voltage VDS.The characteristics may be flat, to indicate that the output resistance become very high. So, it gives the linear region or the Ohomic region of the characteristic. Thus the drain current is less sensitive to variations in drain voltages, which is a very useful feature for application of electronics device in circuits industry. In the case of PMOS for a given negative VGS, the drain voltage is made slightly negative with respect to the source. A current flows from the source to the drain through the conducting channel.

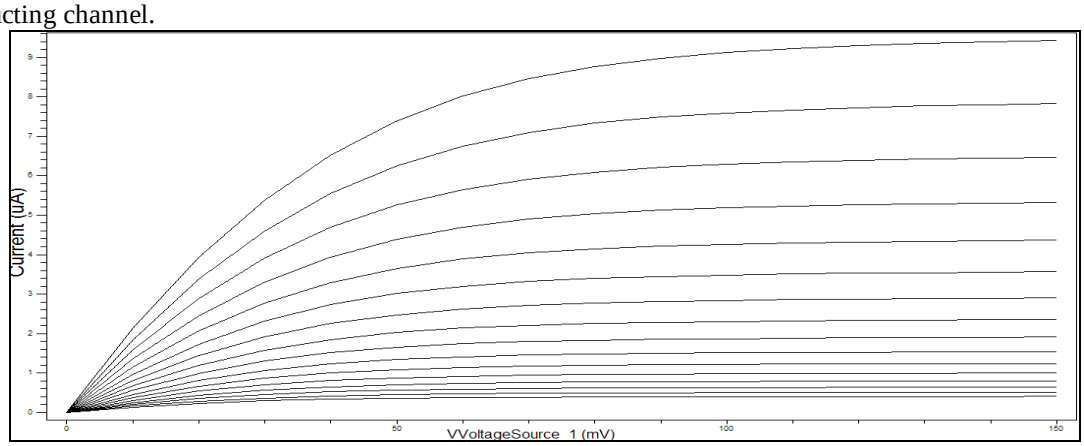

Fig.2. Output characteristic of VTNMOS

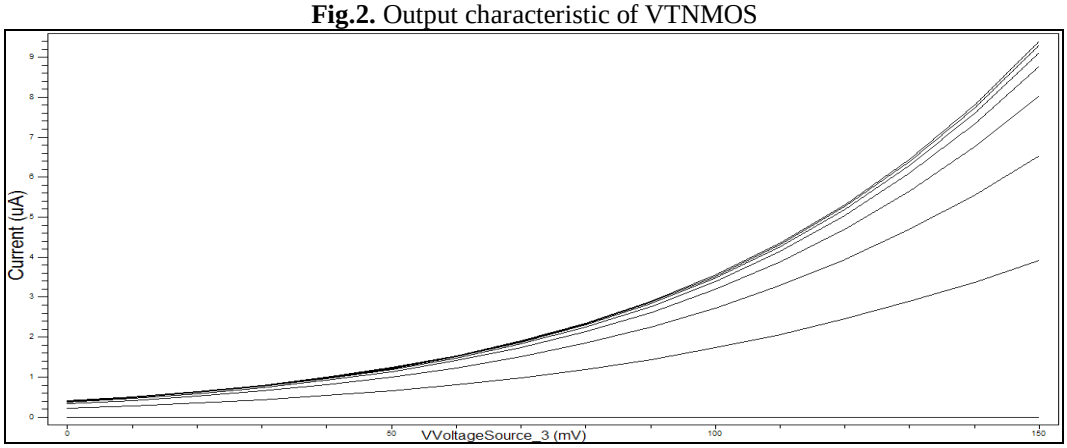

Fig.3. Input characteristic of VTNMOS

2.2 Circuit Techniques

The transistors for VTMOS logic are implemented in 45 nm technology. The threshold voltage for these devices is 150mV for VTNMOS and-150mV for VTPMOS. The Width of VTNMOS (W_N) is chosen as 0.135µm and VTPMOS (W_P) is chosen as 0.27µm. The supply voltage is taken as 0.1V which is below the threshold of both the devices. When the bias voltage is increased beyond supply voltage, the logic levels are affected. Hence there is a limitation for bias voltage and it should be always below supply.

2.3 Braun Multiplier

Braun multipliers are regularly arranged arrays that have n (n-1) adders and n^2 AND gates, where in is the number of inputs. Each of the inputs A and B of the multiplier cell's product bits is generated in parallel with the AND gates. The partial products can be added to the previous sum of the partial product by using one row of an Adder. The carry signals are shifted one bit to the left and then added to the sums of the first adder and the new partial product. They are then passed diagonally downward to the next adder stage. There is no horizontal carry propagation for the first rows. Instead, the carry bit is saved for the subsequent adder stage. A 4 bit Braun Multiplier is shown in Fig 4 given bellow.

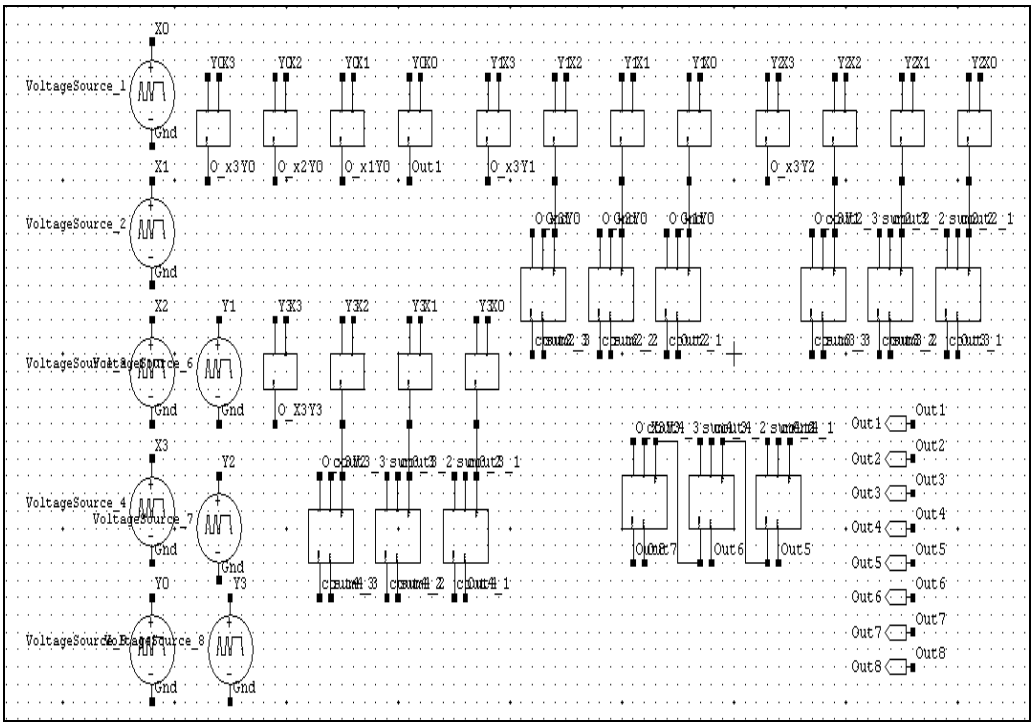

Fig.4. Tanner Spice Diagram and of 4 bit Braun Multiplier

2.4 Baugh Wooley Multiplier

Baugh Wooley Two's compliment Signed multipliers is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits. Baugh Wooley Multiplier is used for both unsigned and signed number multiplication. Signed Number operands which are represented in 2's complemented form. Partial Products are adjusted such that negative sign move to last step, which in turn maximize the regularity of the multiplication array. Baugh Wooley Multiplier operates on signed operands with 2's complement representation to make sure that the signs of all partial products are positive. The basic blocks are constructed by Grey Cell and White cell. In case of White Cell a AND gate and a Full Adder is used and in case of Grey Cell the AND gate is replaced by a NAND Gate.

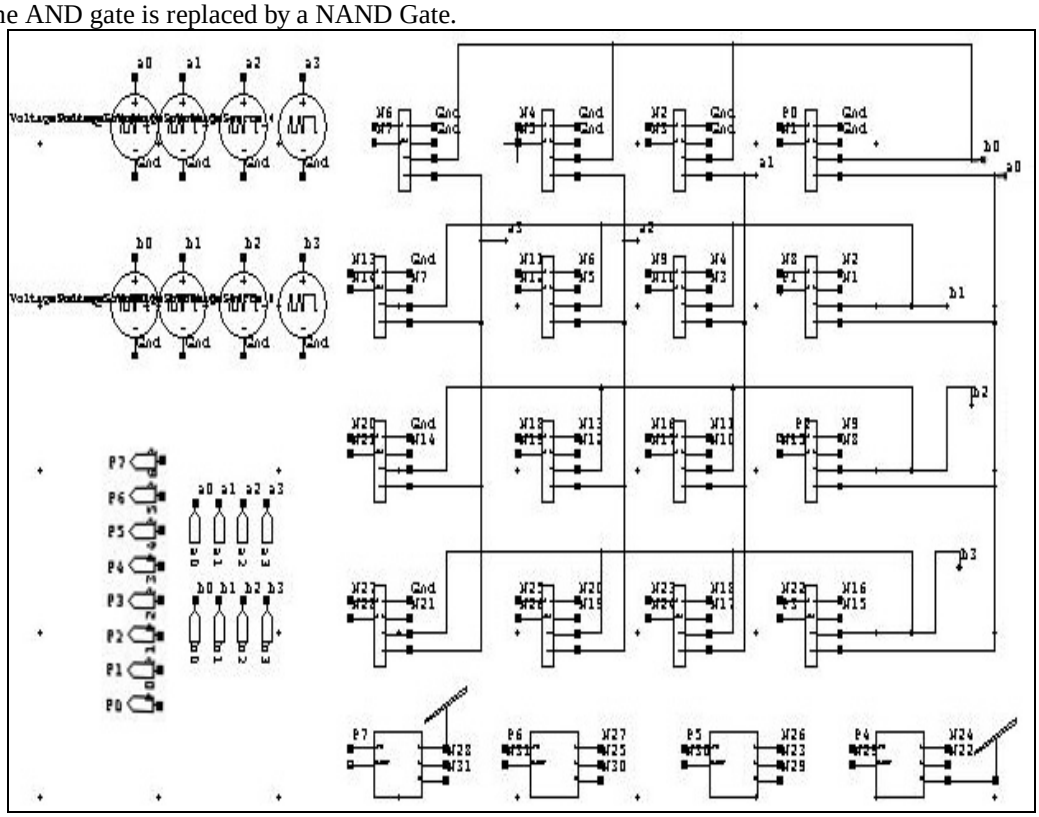

Fig.5.Tanner Spice Diagram and of 4 bit Baugh Wooley Multiplier

2.5 Vedic Multiplier

Urdhva-Tiryakbhyam sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "vertically and crosswise". The main advantage of utilizing this algorithm in comparison with the existing multiplication techniques is the fact that it utilized only logical AND operation, Half address, Full address to complete the operation. Also the partial products required for multiplication are generated in parallel and a priori to the actual addition thus saving as lot of processing time. We have designed 4x4 Vedic multiplier using the Vedic Sutra. Let us see the algorithm first for that we have considered two no's as usual A (1111) and B (1111).

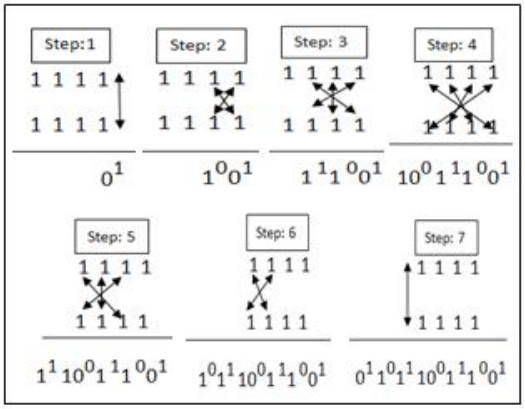

Fig.6.Steps regarding 4x4 Multiplication using Urdhva Tiryakbhyam sutra

Now the result comes like 011011100111001.For getting the final result we here used two arrows one sided arrow shows the final result and both sided arrow shows the intermediate stage and we have numbered each step using Alphabets and for marking addition we have used the + sign Fig.7 shows the complete steps for addition and result.

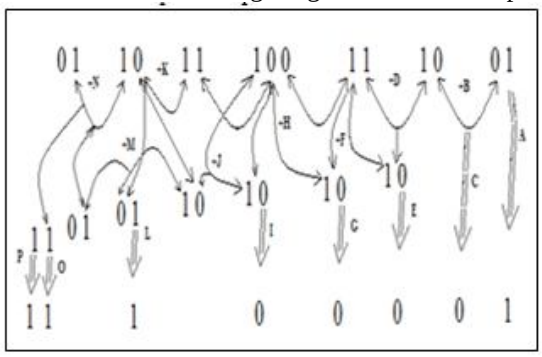

Fig.7. Final Steps regarding 4x4 Vedic Multiplication

3. RESULT ANALYSIS

The Multipliers with VTMOS is simulated in 45nm Technology. The threshold voltage of NMOS in 45nm Technology 0.15V and for PMOS it is -0.15V.The Vdd is taken as 0.1V. The frequency of operation is taken as 1000 MHz.The noise power delay has been calculated with the given specification. The Hardware has also been tested in XILINX 10.1.

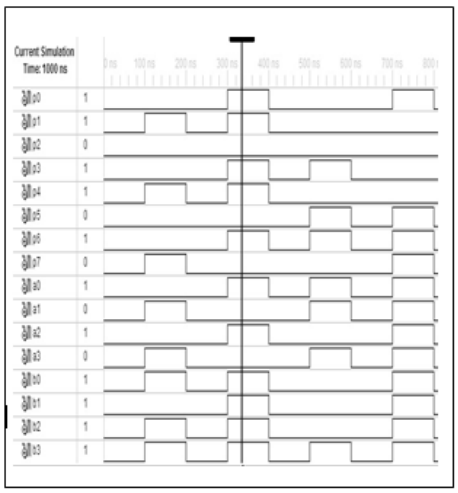

Fig.8. VHDL Output Of Braun Multiplier

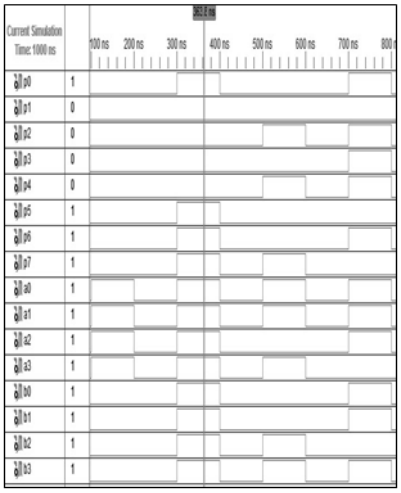

Fig.9. VHDL Output of Vedic Multiplier

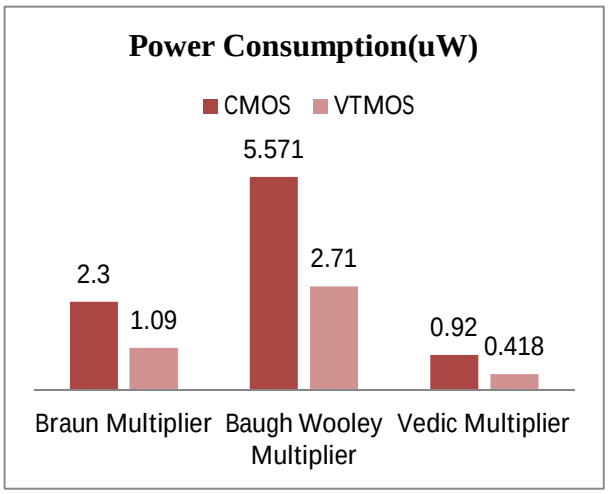

Fig.10. Power Consumption Comparison of Multipliers

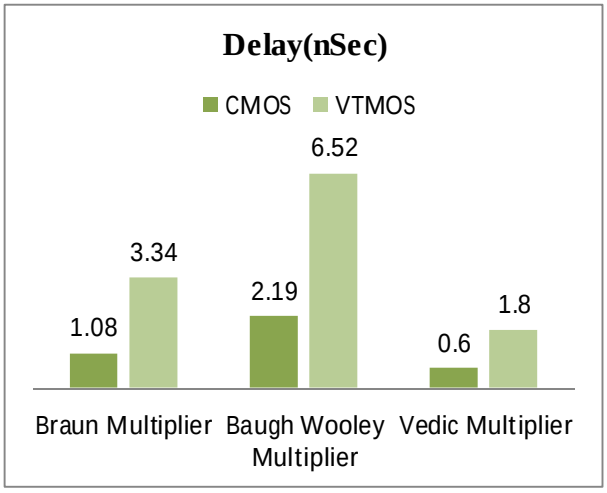

Fig.11. Delay Comparison of Multipliers

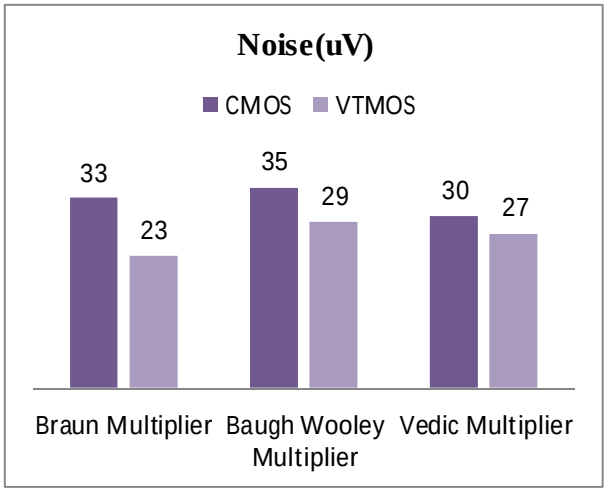

Fig.12. Noise Comparison of Multipliers

4. CONCLUSION

In the era of low power and fast electronics devices speed and power consumption is the major factor of modern industry. Multiplication is one of the most important operations in digital computer systems because the performance of processors is significantly influenced by the speed of their multipliers and adders. A high speed multiplier following the algorithm of Urdhva Tiryakbhyam sutra of Vedic mathematics and using less number of transistors of the basic block of the multiplier we designed the circuits, for reducing the power and increase the speed. Designing these multiplier block or other circuits using CMOS makes it more power consumable blocks. VTMOS logic circuit techniques compared to CMOS circuits is extensively applied due to the low power consumption characteristic. From the result analysis we see, though it has little bit extra delay rather than normal CMOS or DTMOS, but it's this disadvantage overcome by its extreme ultra low power region operating zone, which leads to cost effective circuit.

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