C-V Characteristic of $(PbO)_{1-x}$ $(CdO)_x$/p-Si Heterojunction Prepared by Spray Pyrolysis Technique

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ABSTRAC

Nano particles of Mixed $(PbO)_{1-x}(CdO)_x$ thin films were prepared by spray pyrolysis technique on silicon at a substrate temperature of 400oC. The C-V measurements of this films show that the capacitance decreases with increasing of the reverse bias voltage. The depletion width decreasing with increasing (x), which is due to the increasing in the carrier concentration which leads to a increasing of the capacitance. The built–in voltage increases with increasing of Vol.% of (x). Add CdO lead to improved properties of PbO thin films.

Keywords: Spray pyrolysis, Lead oxide, cadmium oxide, C-V measurements, built–in voltage, depletion width, Thin films.

1. INTRODUCTION

PbO and CdO are an n-type semiconductor materials. Because of its good adsorptive properties and chemical stability, it can be deposited onto glass, ceramics, oxides, and substrate materials of other types. It has a high melting point and good transmission, and does not easily react with oxygen and water vapor in the air, so it has a high specific volume and good cycling performance. In addition, PbO and CdO thin films are also used for film resistors, electric conversion films, heat reflective mirrors, semiconductor– insulator–semiconductor (SIS) heterojunction structures, and surface protection layers of glass. At present, its most common application is as the anode material of solar cells [1,2]. Varieties of methods like dc reactive sputtering, chemical bath deposition [3], activated reactive evaporation [4], solution growth [5], thermal oxidation [6], sol–gel [7], and spray pyrolysis [8,9] have been reported in the preparation of CdO and PbO thin films. The electro optical properties of CdO make this material very convenient as a solar cell material [1]. In attempts to improvise the properties of PbO, it is being tried out to mix with other oxides. Recently, Hosono *et al.* [10] reported amorphous semiconductor $2CdO{\cdot}PbO_x$ thin films with a novel information about the carrier generation through the formation of oxygen vacancies. In this paper, the focus is on capacity measurements effort films prepared as one of the important measurements which we can determine the type of heterojunction (abrupt or graded), built in voltage (V_{bi}), carrier concentration and finally the width of depletion layer.

2. EXPERIMENTAL DETAILS

A simple homemade spray pyrolysis experimental setup was employed to prepare mixed $(PbO)_{1-x}(CdO)_x$ thin films on silicon[p-type,(111) orientation and (1×1 cm^2) diameter] at a substrate temperature of 400 °C. The difference in CdO vol.% (x) was achieved by mixing the aqueous solutions of 0.1 M of lead and cadmium acetates to pre-determined volume ratio. The value of (x) in the solution was varied from 0.00 to 1.00 (x=0, 0.2, 0.4, 0.6, 0.8, 1). The mixed solutions which were then diluted with water formed the final spray solution and a total volume of 25 ml was used in each deposition. The deposition parameters such as spray nozzle-substrate distance (30 cm), ,spray time (4 s) and the spray interval (1 min) were kept constant. The carrier gas (filtered compressed air) flow rate was maintained at 6 l/min at a pressure of 6.5×10^4 Nm^{-2}. The capacitance of the heterojunction was measured as a function of the reverse bias voltage in the range (0 – 1) volt with fixed frequency of 1MHz by using HP-R2C unit model 4274A and 4275A multi-frequency LRC meter.

3. RESULTS AND DISCUSSION

The variation of capacitance as a function of voltage in the range of (0-1) Volt and reverse bias voltage in the range of (0 - ¯1) Volt and at frequency equal to 1 MHz has been studied, for $(PbO)_{1-x}$ $(CdO)_x$/p-Si heterojunction at different vol.% of (x), as shown in Figure (1) and Figure (2). It is clear that the capacitance decreases with increasing of the reverse bias voltage, and the decreasing was non-linear. Such behavior is attributed to the decreasing in the depletion region width, which leads to increase of the value of a built– in voltage. An enhancement of the capacitance of zero bias voltage (C_o) with the increasing of Vol.% of CdO could be shown in the table (1). This behavior attributed to the surface states which leads to a decrease in the depletion layer and an increasing of the capacitance. The width of depletion layer can be calculated using equation :

$$W = \frac{\varepsilon_s A_j}{C_o} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (1)$$

Has C_o been the capacitance at zero biasing voltage, A_j is the effective area of the junction and ε_s is the permittivity of semiconductor calculated from the equation [11]:

$$\varepsilon_s = \frac{(\varepsilon_1 \varepsilon_2)}{(\varepsilon_1 + \varepsilon_2)} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (2)$$

Where ε_1 and ε_2 is the semiconductor permittivity of the two semiconductor materials. We can notice from Table (1) that the depletion width decreasing with increasing (x), which is due to the increasing in the carrier concentration which leads to a increasing of the capacitance .The inverse capacitance square is plotted against applying a reverse bias voltage for $(PbO)_{1-x}$ $(CdO)_x$/p-Si heterojunction at different at different Vol.% of (x), as shown in Figure (3). The plots revealed straight line relationship which means that the junction was of an abrupt type. This is in agreement with the results of [12].The interception of the straight line with the voltage axis at ($1/C^2 = 0$), represents the built–in voltage [13]. We observed from Table (1) that the built–in voltage increases with increasing of Vol.% of CdO.

From the same Figure(3), we have deduced the carrier's concentration of the abrupt $(PbO)_{1-x}$ $(CdO)_x$/Si heterojunction at different Vol.% of (x), from the slope of the straight line by using equation [14] :

$$C^2 = \frac{q N_D N_A \varepsilon_1 \varepsilon_2}{2(N_A \varepsilon_1 + N_D \varepsilon_2)} \cdot \frac{1}{(V_{bi} - V)} \quad \dots\dots\dots\dots\dots\dots\dots\dots (3)$$

Here, N_D and N_A is the donor density in n-type, the acceptor density in p-Si, ε_1 and ε_2 are the dielectric constants of n-type and p-Si, respectively, V_{bi} is the built – in junction potential, and V is the applied voltage. Table (1) exhibits that these values which increase with increasing (x) .

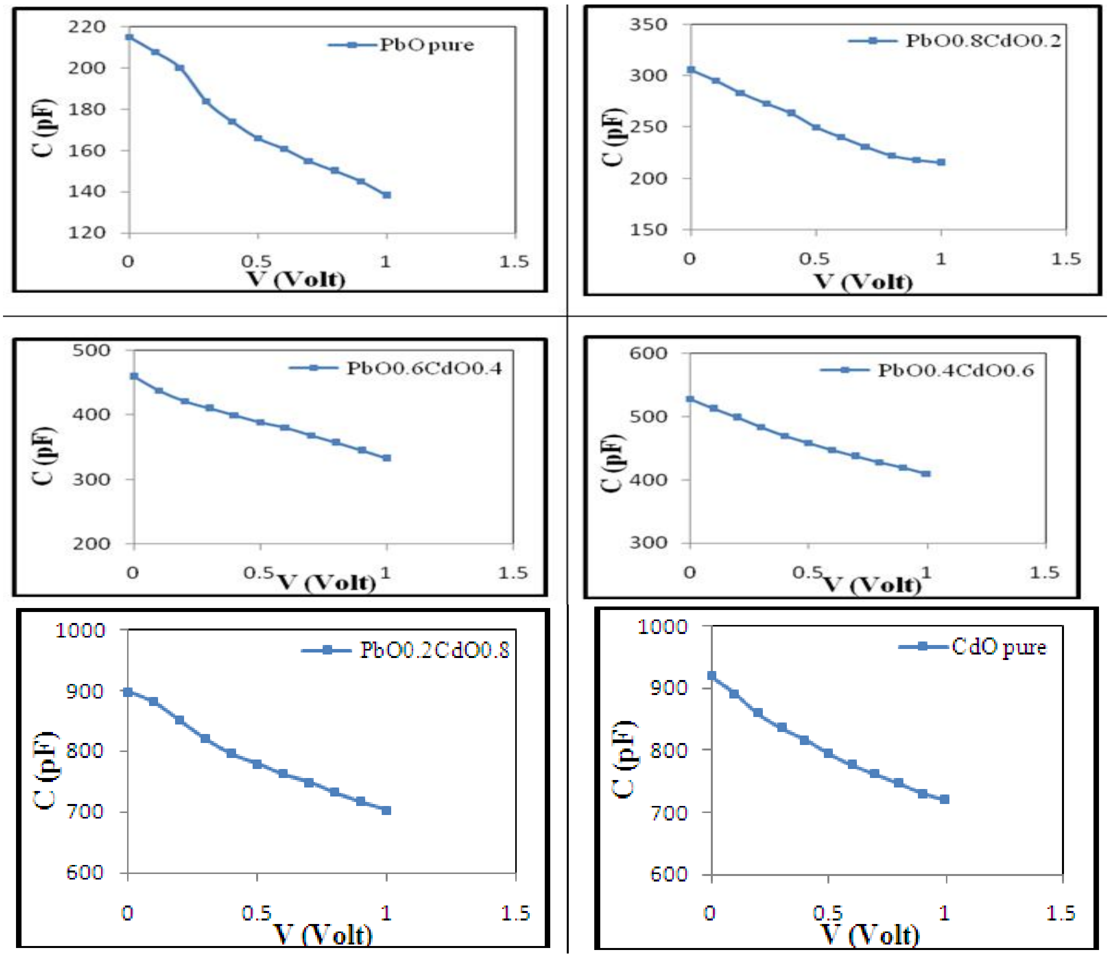


Figure (1): The variation of capacitance as a function of voltage for for $(PbO)_{1-x}$ $(CdO)_x$ films at different Vol.% of (x).

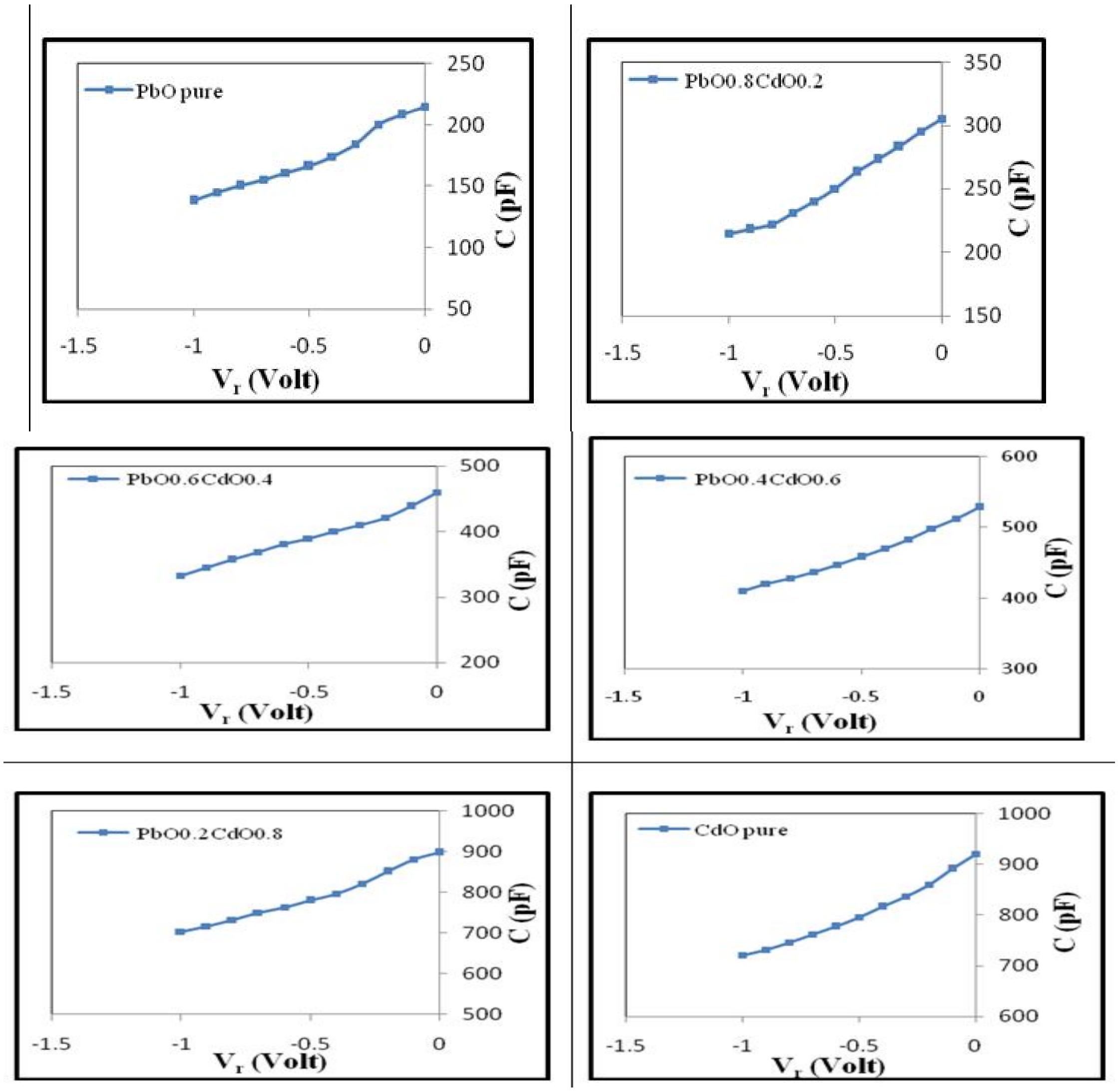
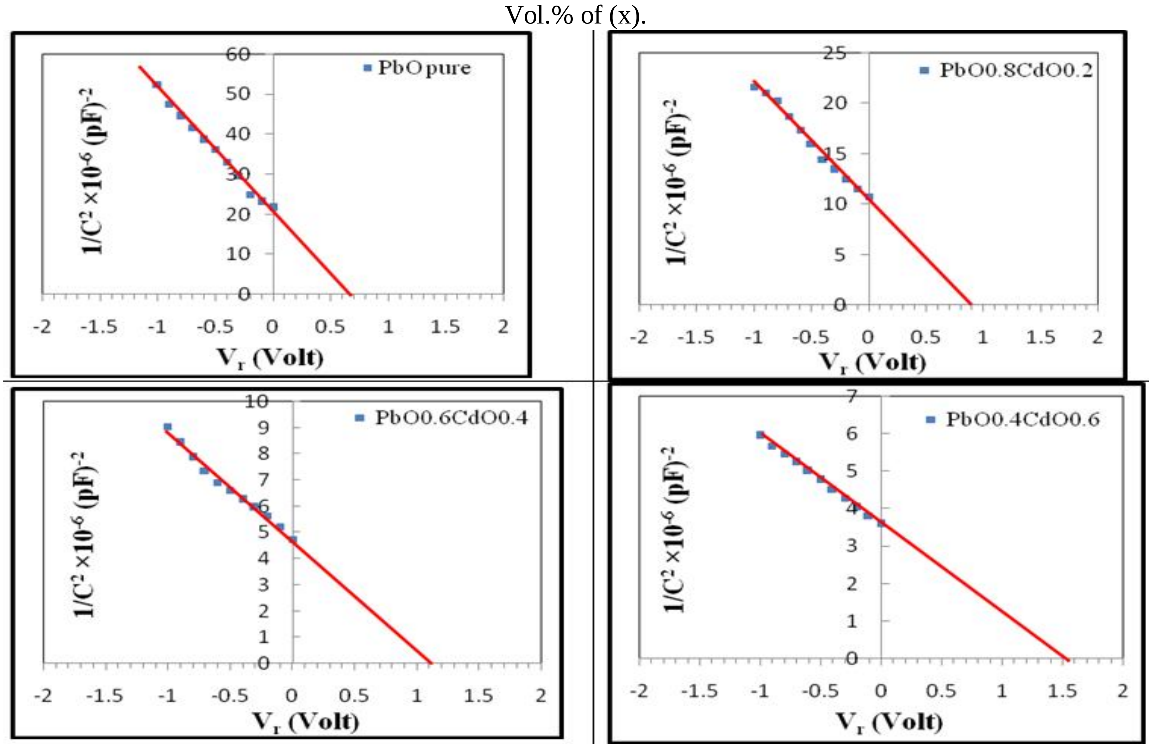


Figure (2): The variation of capacitance as a function of reverse bias voltage for $(PbO)_{1-x}$ $(CdO)_x$ films at different Vol.% of (x).



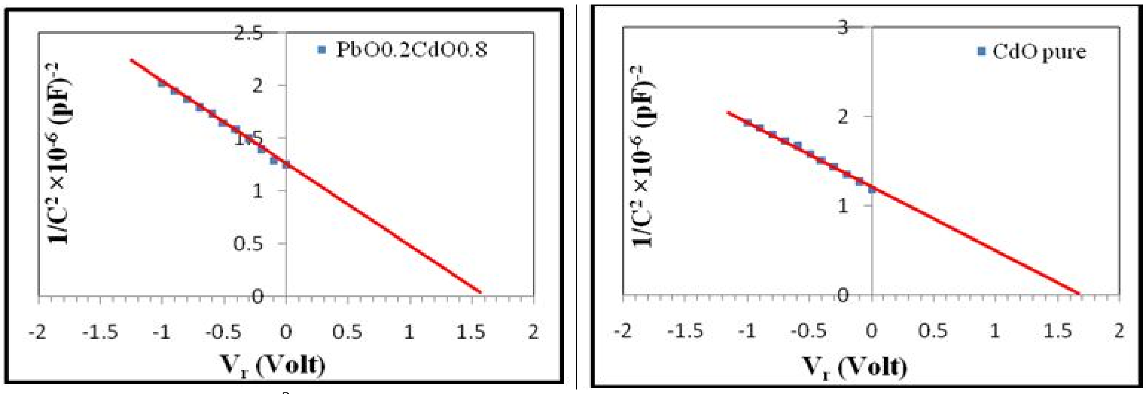


Figure (3): The variation of $1/C^2$ as a function of reverse bias voltage for $(PbO)_{1-x}$ $(CdO)_x$ films at different Vol.% of (x).

Table (1): The variation of the C_o ,W ,V_{bi}, and N_D for for $(PbO)_{1-x}$ $(CdO)_x$ films at different Vol.% of (x).

Sample	**C_o (pF)**	**W (μm)**	**V_{bi} (Volt)**	**N_D (cm^{-3})**
PbO $_{pure}$	215	0.0375	0.7	1.23×10^{11}
$PbO_{0.8}CdO_{0.2}$	305	0.0247	0.9	3.12×10^{11}
$PbO_{0.6}CdO_{0.4}$	459	0.0148	1.1	4.05×10^{12}
$PbO_{0.4}CdO_{0.6}$	528	0.0109	1.5	0.14×10^{15}
$PbO_{0.2}CdO_{0.8}$	897	0.464×10^{-2}	1.6	2.79×10^{17}
CdO $_{pure}$	920	1.5299×10^{-3}	1.7	0.63×10^{20}

4. CONCLUSION

$(PbO)_{1-x}(CdO)_x$ mixed films were deposited on silicon substrates at 400 °C and studied as a function of CdO vol.%, x(0≤x≤1). The C-V measurements of this film show that the capacitance decreases with increasing of the reverse bias voltage, and the decreasing was non-linear. The depletion width decreasing with increasing (x), which is due to the increasing in the carrier concentration which leads to a increasing of the capacitance. The built–in voltage increases with increasing of Vol.% of CdO.

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