International Journal of Application or Innovation in Engineering & Management (IJAIEM)
Web Site: www.ijaiem.org Email: editor@ijaiem.org
Volume 4, Issue 3, March 2015 ISSN 2319 - 4847

VLSI Designing of High Speed Parallel Multiplier –Accumulator Based On Radix4 Booths Multiplier

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ABSTRACT

In this paper, we proposed a new architecture of multiplier-and-accumulator (MAC) for high-speed arithmetic. By combining multiplication with accumulation and devising a hybrid type of ripple carry adder (RCA), the performance was improved. Since the accumulator that has the largest delay in MAC was merged into RCA, the overall performance was elevated. Radix 4 modified Booth algorithms can be utilized for reduction of the partial products. The parallel multiplier like radix 4 modified booth multiplier accomplishes the computations utilizing fewer adders and less iterative steps. Based on the simplification of addition operation and power reduction property in ripple carry adder (RCA),a low power radix 4 modified booth multiplier is proposed, compared with the radix 4 modified booth multiplier using carry look ahead adder(CLA),the experimental result shows that our propose design has reduce the Delay of circuit to 6.21 % using RCA, Area has estimated as 947 which was 1141 when designed with CLA Adder.

Keywords: Booth multiplier, Low power, Modified Booth Multiplier, Multiplication, Partial Product Generation (PPG), RCA, VHDL.

1. INTRODUCTION

With the recent rapid advances in multimedia and communication systems, real-time signal processing like audio signal processing, video/image processing, or large-capacity data processing are increasingly being demanded. The multiplier and multiplier-and-accumulator (MAC) [1] are the essential elements of the digital signal processing such as filtering, convolution, and inner products. The energy efficient digital signal processing (DSP) modules are becoming increasingly important in wireless sensor networks, where from tens to thousands of battery-operated micro sensor nodes are deployed remotely and used to relay sensing data to the end-user in these application/systems, a multiplier is a fundamental arithmetic unit and widely used in circuits. The speed of multiply operation is of great importance in digital signal processing as well as in the general purpose processors today, especially since the media processing took off. In the past multiplication was generally implemented via a sequence of addition, subtraction, and shift operations. Multiplication can be considered as a series of repeated additions. The number to be added is the multiplicand, the number of times that it is added is the multiplier, and the result is the product. Each step of addition generates a partial product. In most computers, the operand usually contains the same number of bits. When the operands are interpreted as integers, the product is generally twice the length of operands in order to preserve the information content. This repeated addition method that is suggested by the arithmetic definition is slow that it is almost always replaced by an algorithm that makes use of positional representation. It is possible to decompose multipliers into two parts. The first part is dedicated to the generation of partial products, and the second one collects and adds them. Booth multiplication is used greatly to increase the speed of the multiplier by encoding the numbers that are multiplied.

This is a standard technique used in chip design and provides significant improvements over the long multiplication technique. In the conventional multiplier, the number of partial products to be added are determined by the number of bits the multiplier or multiplicand being used. The bigger the number of bits the multiplicand or the multiplier contain, the longer time it takes to produce the product. The delay of multiplier is determined largely by the number of partial products to be added. One of the most popular algorithms used to reduce the number of partial products is Booth Encoding multiplier. Booth Encoding multiplication is able to reduce the number of partial products being encoded to increase the speed of the binary multiplications. Radix-4 Booth Encoding multiplier reduces the number of partial products by half, N/2. [2] This is able to increase the time of compression and contribute to an increase in speed. [3] It was then taken a step further in this analysis by designing and synthesizing Radix-8 Booth Encoding multiplier, Radix-16 Booth Encoding multiplier and Radix-32 Booth Encoding multiplier to determine if the speed reduces or the area increases as the higher the radix-based multiplier designs are. The number of partial products reduces as the Radix-based Booth Encoding multipliers increase higher. Radix-8 Booth Encoding multiplier will encounter a reduction of

N/3 in the partial products while Radix-16 Booth Encoding multiplier reduces its number of partial product by N/4. Radix-32 Booth Encoding multiplier reduces the number of partial products even more by a reduction of N/5. The algorithm to produce the partial products gets a lot more complicated as the higher the Radix-based Booth Encoding multiplier.

In booth multiplier the number of summands is reduced by recording the multiplier bit into groups that select multiplies of multiplicand. From the basics of Booth Multiplication it can be proved that the addition/subtraction operation can be skipped if the successive bits in the multiplicand are same. To achieve high performance, the modified Booth encoding which reduces the number of partial products by a factor of two through performing the multiplier recoding has been widely adopted in parallel multipliers. The multiplication operations have the fixed-width property. That is, their input data and output results have the same bit width. For example, the (2W - 1)-bit product obtained from W-bit multiplicand and W-bit multiplier is quantized to W-bits by eliminating the (W - 1) least-significant bits (LSBs). In typical fixed-width multipliers, the adder cells required for the computation of the (W - 1) LSBs are omitted and appropriate biases are introduced to the retained adder cells. The hardware complexity reduction and power saving can be achieved by directly removing the adder cells of standard multiplier. Due to this a huge truncation error will be introduced. To effectively reduce the truncation error, various error compensation methods, which add estimated compensation value to the carry inputs of the reserved adder cells. The error compensation value can be produced by the constant scheme or the adaptive scheme. The adaptive error compensation approaches are developed only for fixed-width array multipliers and cannot be applied to significantly reduce the truncation error of fixed-width modified Booth multipliers directly. To overcome this problem, several error compensation approaches have been proposed to effectively reduce the truncation error of fixed-width modified Booth multipliers. To obtain better error performance with a simple error compensation circuit, Booth encoded outputs are utilized to generate the error compensation value.

2. LITERATURE REVIEW

Young-Ho Seo and Dong-Wook Kim has designed proposed a new architecture of multiplier-and-accumulator (MAC) for high-speed arithmetic. By combining multiplication with accumulation and devising a hybrid type of carry save adder (CSA), the performance was improved. Since the accumulator that has the largest delay in MAC was merged into CSA, the overall performance was elevated.

Now, this paper, a new architecture for a high-speed MAC is proposed. In this MAC, the computations of multiplication and accumulation are combined and a hybrid-type CSA structure is proposed to reduce the critical path and improve the output rate. It uses MBA algorithm based on 1’s complement number system. A modified array structure for the sign bits is used to increase the density of the operands. A carry look-ahead adder (CLA) is inserted in the CSA tree to reduce the number of bits in the final adder. In addition, in order to increase the output rate by optimizing the pipeline efficiency, intermediate calculation results are accumulated in the form of sum and carry instead of the final adder outputs. Zn = -2* Bn+1 + Bn + Bn-1, PPG is the combination circuit of the product generator and the 5 to 1 MUX circuit. Product generator is designed to produce the product by multiplying the multiplicand A by 0, 1, - 1, 2 or -2. A 5 to 1 MUX is designed to determine which product is chosen depending on the M, 2M, 3M control signal which is generated from the MBE. Now, for product generator, multiply by zero means the multiplicand is multiplied by “0”.Multiply by “1” means the product still remains the same as the multiplicand value. Multiply by “-1” means that the product is the two's complement form of the number. Multiply by “-2” is to be shifted left one bit the two's complement of the multiplicand value and multiply by “2” means just shift left the multiplicand by only one place. In this paper, a new MAC architecture to execute the multiplication- accumulation operation, which is the key operation, for digital signal processing and multimedia information processing efficiently, was proposed. By removing the independent accumulation process that has the largest delay and merging it to the compression process of the partial products, the overall MAC performance has been improved almost twice as much as in the previous work.

Shaikh Kalisha Baba and D.Rajaramesh has design and implementation of Advanced Modified Booth Encoding (AMBE) multiplier for both signed and unsigned 32 - bit numbers multiplication. The already existed Modified Booth Encoding multiplier and the Baugh-Wooley multiplier perform multiplication operation on signed numbers only.

Whereas the array multiplier and Braun array multipliers perform multiplication operation on unsigned numbers only. Thus, the requirement of the modern computer system is a dedicated and very high speed unique multiplier unit for signed and unsigned numbers. Therefore, this paper presents the design and implementation of AMBE multiplier. The modified Booth Encoder circuit generates half the partial products in parallel. By extending sign bit of the operands and generating an additional partial product the AMBE multiplier is obtained. The Carry Save Adder (CSA) tree and the final Carry Look ahead (CLA) adder used to speed up the multiplier operation. Since signed and unsigned multiplication operation is performed by the same multiplier unit the required hardware and the chip area reduces and this in turn reduces power dissipation and cost of a system. The high speed Booth multipliers and pipelined Booth multipliers are used for digital signal processing (DSP) applications such as for multimedia and communication systems. High speed DSP computation applications such as Fast Fourier transform (FFT) require additions and multiplications. The conventional modified Booth encoding (MBE) generates an irregular partial product array because of the extra partial product bit at the least significant bit position of each partial product row. The requirement of the modern computer system is a dedicated and very high speed multiplier unit that can perform multiplication operation on signed as well as unsigned numbers. In this paper they designed and implemented a dedicated multiplier unit that can perform multiplication operation on both signed and unsigned numbers, and this multiplier is called as AMBE multiplier. The main goal of this paper is to design and implement 32×32 multiplier for signed and unsigned numbers using MBE technique. Using the MBE logic and considering other conditions the Boolean expression for one bit partial product generator. The SUMBE multiplier does not separately consider the encoder and the decoder logic, but instead implemented as a single unit called partial product generator. The negative partial products are converted into 2□s complement by adding a negate (Ni) bit. The required signed extension to convert 2's complement signed multiplier into both signed-unsigned multipliers.

In this paper, they present a 32-bit×32-bit advanced multiplier capable of carrying out both signed and unsigned operations. The proposed novel unified signed/unsigned multiplier was optimized in terms of speed, power consumption and silicon area by exploiting more regular partial product array, developing more efficient compression methods and combining several types of fast adders.

3. METHODOLOGY

Multipliers are important operands and utilize in high-speed low-power systems where a large amount of information is to be calculated. The modified Booth algorithm reduces the number of partial products by half. The modified Booth encoding (MBE) scheme is known as the most efficient Booth encoding and decoding scheme. To multiply, multiplicand „X□ by multiplier „Y□ using the modified Booth algorithm. First group the multiplier bits „Y□ by three bits and encoding into one of {-2, -1, 0, 1, 2}. Prior to convert the multiplier, a zero is appended into the Least Significant Bit (LSB) of the multiplier. Table I shows the rules to generate the encoded signals by MBE scheme and Fig. 1 shows the corresponding logic diagram. The Booth decoder generates the partial products using the encoded signals as shown in Fig. 2.

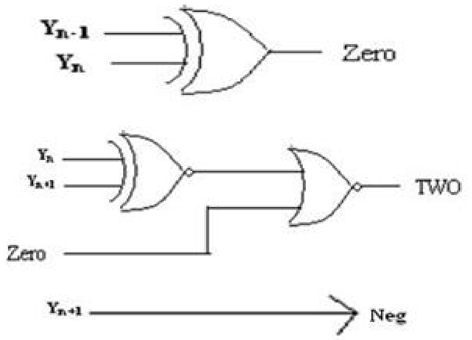


Fig 1. Booth encoder

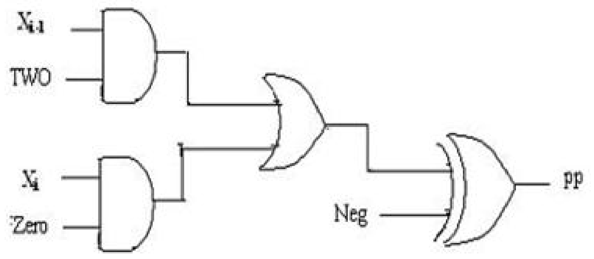


Fig 2. Booth decoder.

Table1: Truth table for modified booth encoder.

Y_{n+1}	Y_n	Y_{n-1}	Z_n	Operate	Neg	Zero	Two
0	0	0	0	0	0	0	0
0	0	1	1	1 x M	0	1	0
0	1	0	1	1 x M	0	1	0
0	1	1	2	-2 x M	0	0	1
1	0	0	-2	-2 x M	1	0	1
1	0	1	-1	-1 x M	1	1	0
1	1	0	-1	-1 x M	1	1	0
1	1	1	0	0	0	0	0

In an n-bit modified Booth multiplier, the number of Booth encoders is n/2 and the number of partial product generator (PPG) circuits is approximately n2, hence power consumption and die area in the Booth section is dominated by PPG. So, integration of PPG (Booth Decoder) section is more important than Booth encoder (BE) block. The conventionally used modified Booth selector computes the partial product of jth bit and ith row by using the equation1.

PPij = (Xj. X1_2+Xj-1.X1_1) XOR Neg (1)

Where Xj and Xj-1 are the multiplicand inputs of weight 2j and 2j-1 respectively, X1_2 and X1_1 determine whether the multiplicand should be doubled or not and Neg is a digit which determines if the multiplicand should be inverted or not. Booth recoding is fully parallel and carry free. It can be applied to design a tree and array multiplier, where all the multiples are needed at once. Radix-4 Booth recoding system works perfectly for both signed and unsigned operations.

Proposed Methodology:

As it has been found that, Booth Wallace multiplier is most efficient among all, giving optimum delay, with lesser power and small chip area for multiplication. Therefore the proposed design for low power high speed Booth multiplier and its implementation on reconfigurable hardware will utilize the carry ripple adder along with the booth‟ s algorithm to accomplish the goal.

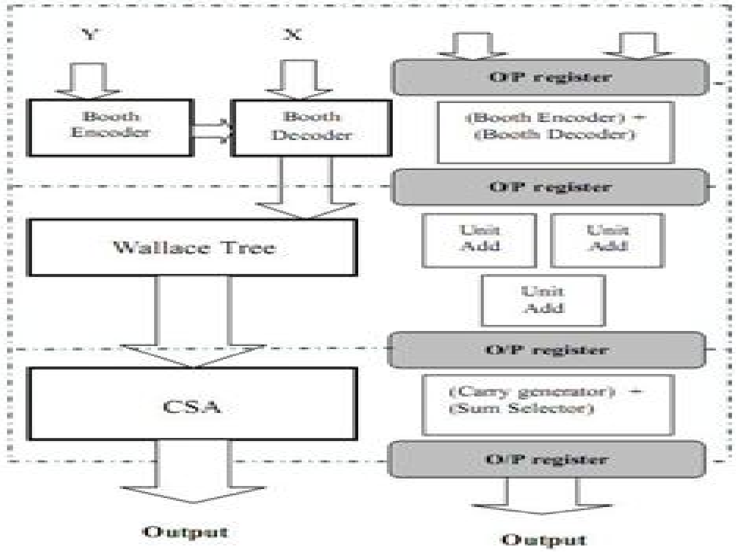
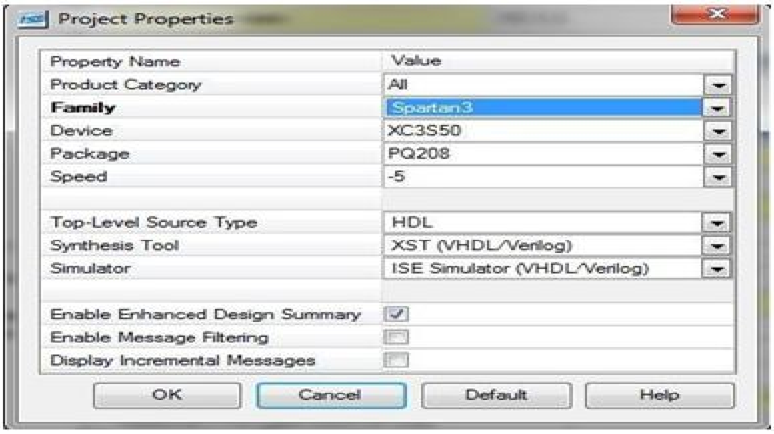


Fig 3. Block diagram of Block Diagram of Modified Booth Multiplier.

4. RESULT

Xilinx 13.1i ISE Simulator has been used to simulate the proposed methodology of multiplication of two 8 bit numbers using Radix-4 modified Booths algorithm. The device used by the simulator is XC3S50 of Spartan3 family with the speed of -5 which is shown in Fig. 4


Project Properties

Property Name	Value
Product Category	All
Family	Spartan3
Device	XC3S50
Package	PQ208
Speed	-5
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISE Simulator (VHDL/Verilog)
Enable Enhanced Design Summary	☑
Enable Message Filtering	□
Display Incremental Messages	□

Fig. 4. Properties of Xilinx 13.1i module

The Result Can be analyze by following table

Table 2. Multiplication of a and b

Input a[7:0]	Input b[7:0]	Classical Booths multiplier Output c [7:0]	Modified Booths multiplier Output c [7:0]
15	105	1575	1575
85	124	10540	10540
92	49	4508	4508
-36	-48	5824	5824
-33	28	6244	-924

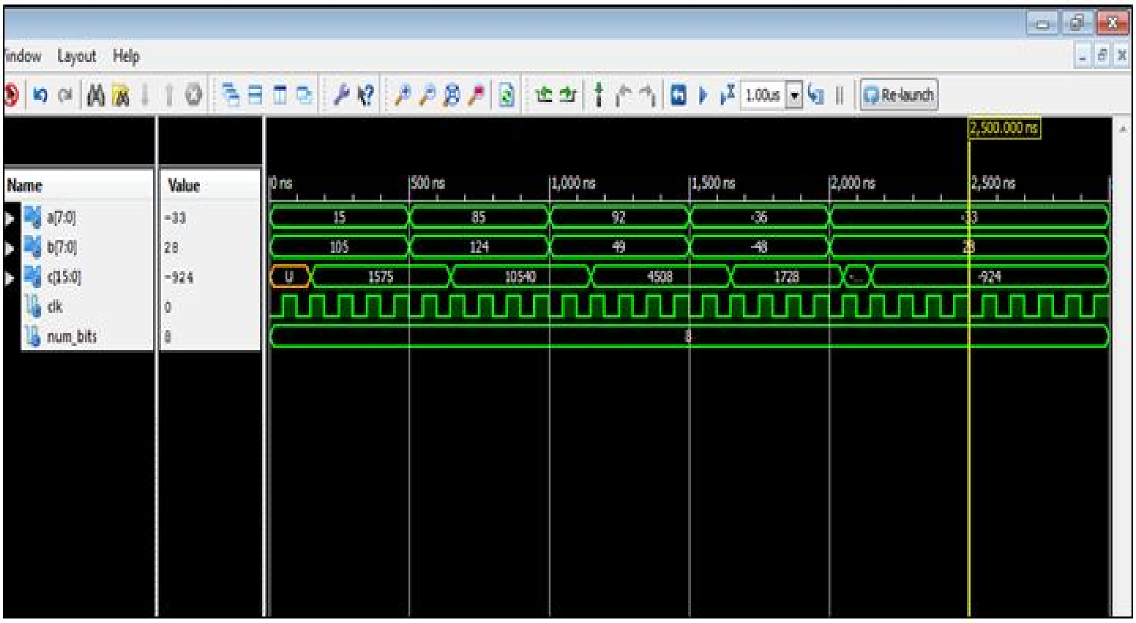
The comparison of the synthesis report of the former results from radix 2 booth multiplier using carry look ahead adder (CLA) and the proposed delay radix 4 booth multiplier using on chip ripple carry adder (RCA) are summarized in the table below:

Table 3.Comparision of CLA & RCA properties

Properties	Radix 2 booth multiplier using CLA	Radix 4 booth Classical multiplier using RCA	Radix 4 Modified booth multiplier using RCA
Device and family	Spartan 2	Spartan 3	Spartan 3
% Delay reduction	22.9%	6.21%	6.21%
Delay (dynamic)ns	28.6ns	6.216ns	6.216ns
Area Estimation of GATE size by synthesis	1141	978	947

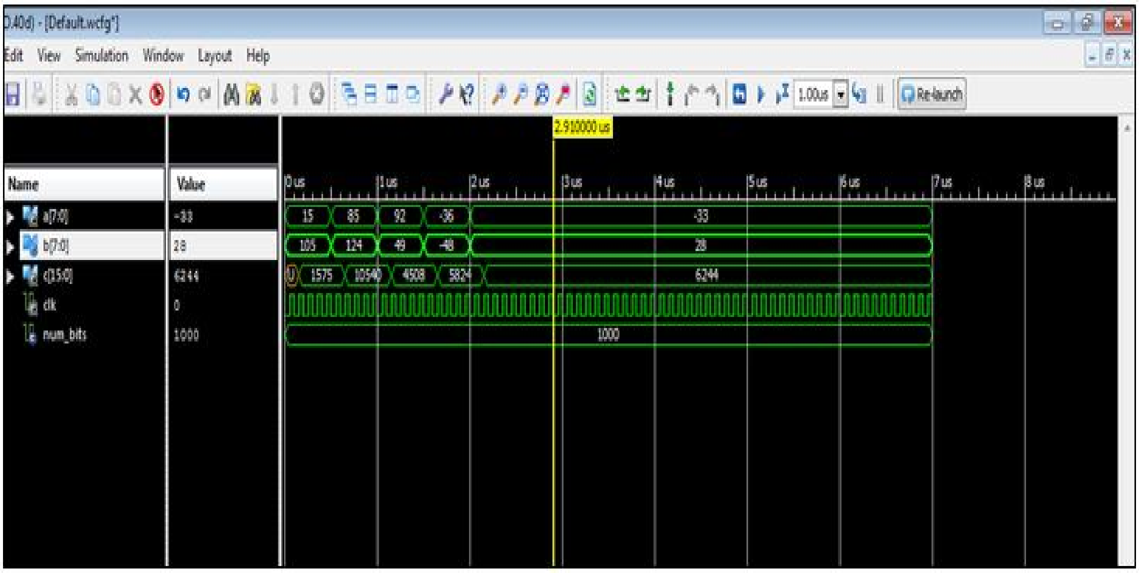
The multiplication operation is performed in many fragments of a digital system or digital computer. Radix_4 modified Booth algorithm can be utilized for reduction of the partial products. The parallel multiplier like radix 4 modified booth multiplier accomplishes the computations utilizing fewer adders and less iterative steps.

Based on the simplification of addition operation and power reduction property in ripple carry adder(RCA),a minimum delay radix 4 modified booth multiplier is proposed, compared with the radix 4 modified booth multiplier using carry look ahead adder(CLA),the experimental result shows that our propose design has reduce the delay to 6.21 % using RCA, Area has estimated as 947 which was 1141 when designed with CLA Adder.



Name	Value
a[7:0]	-33
b[7:0]	28
c[15:0]	-924
clk	0
num_bits	8

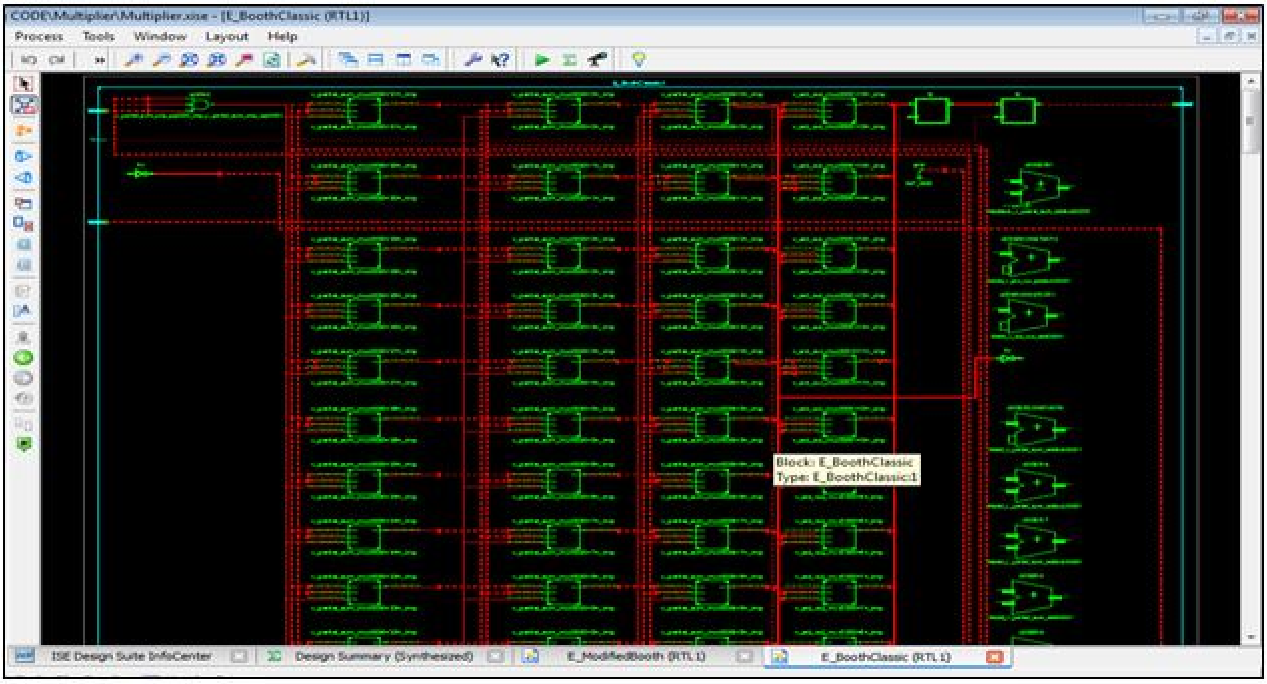
Fig. 5: Simulation results of modified booths multiplication of two 8-bit



Name	Value
a[7:0]	-33
b[7:0]	28
c[15:0]	6244
clk	0
num_bits	1000

Fig.6: Simulation results of Classical booths multiplication of two 8-bit

Figure below shows the RTL schematic of the multiplier using the on chip ripple carry adder for the radix 4 booth multiplier.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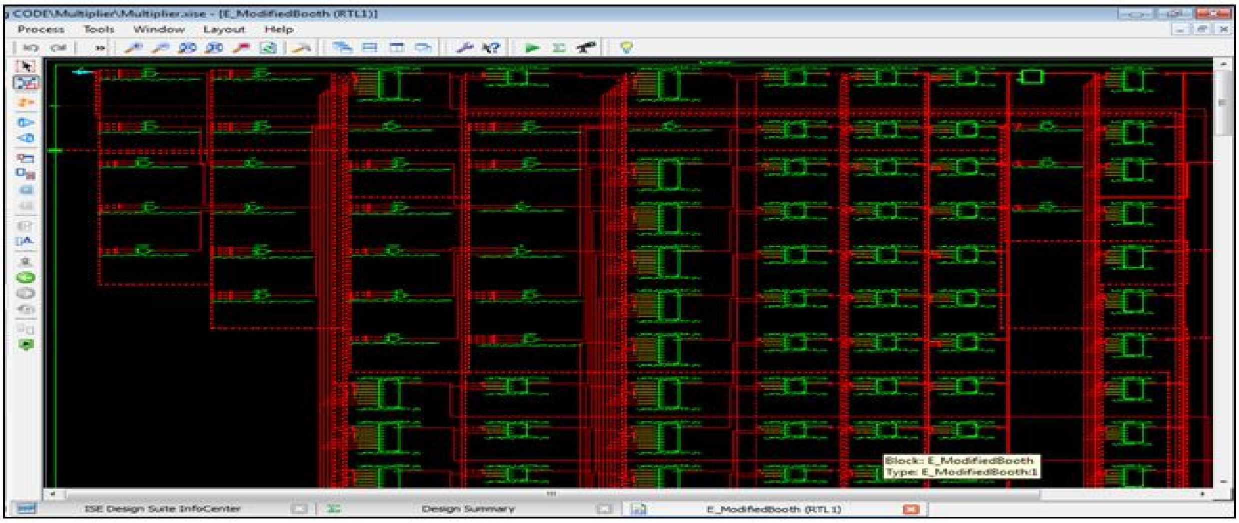
E_ModifiedBooth (RTL 1)
E_BoothClassic (RTL 1)

Fig.7: RTL Schematic of Classical Booth Multipliers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Design Summary
E_ModifiedBooth (RTL 1)

Fig.8: RTL Schematic of Modified Booth Multipliers

5. CONCLUSION

The radix 4 modified booth multipliers using RCA is realized in the VHDL. The analysis shows that time delay proposed by modified Booth's multipliers using RCA is 6.21 ns as compared to the radix 2 Booth's multiplier using CLA which is 28.6 ns. The power occurred is also less as compared to the conventional Booth's multiplier.

Table 4. Comparision of CLA & RCA properties

Properties	Radix 2 booth multiplier using CLA	Radix 4 Modified booth multiplier using RCA
Delay (dynamic)ns	28.6ns	6.216ns
Area Estimation of GATE size by synthesis	1141	947

REFERENCES

[1] J.J.F. Cavanagh, Digital Computer Arithmetic. New York: McGraw-Hill, 1984.

[2] Behrooz Parhami, “Computer Arithmetic: Algorithms and Hardware Designs”, Oxford New York, Oxford University Press, New York, 2000.

[3] C. N.Marimuthu, P. Thangaraj, Anna University, India, “Low Power High Performance Multiplier”, ICGST-PDCS International Conference on Computer Science and Engineering, 2008.

[4] William J. Dally and Steve Lac, "VLSI Architecture: Past, Present, and Future", 20th International Conference on VLSI Design, IEEE, 2005.

[5] Power Simulation and Estimation in VLSI Circuits .University of Southern California Department of EE Systems Los Angeles CA.

[6] Dhireesha Kudithipudi and Eugene John, "Implementation of Low Power Digital Multipliers Using 10 Transistor Adder Blocks", IEEE Journal of Solid State Circuits, Volume 32 , no 12, November 1997.

[7] Poornimam, Shivrajkumar Patil, Shivukumar, Shridhar K. P., Sanjay H., "Implementation of Multiplier using Vedic Algorithm" IJITEE, volume 2 ,issue 6,may 2013.

[8] Kripa Mathew, S. Asha Latha, T. Ravi, E. Logashanmugam, "Design and Analysis of an Array Multiplier Using an Area Efficient Full Adder Cell in 32nm CMOS Technology", The International Journal Of Engineering And Science (Ijes), Volume2, Issue 3,Pages 8-16,2013.

[9] Mr.M.V. Sathish, Mrs. Sailaja, "Vlsi architecture of parallel multiplier– accumulator based on radix-2 modified booth algorithm", International Conference on Field Programmable Logic and Application, 2005.

[10] S. Kiruthika1, R.Nirmal Kumar, Dr S.Valarmathy," Comparative Analysis of 4-Bit Multipliers Using Low Power 8-Transistor Full Adder Cells", International Journal of Emerging Technology and Advanced Engineering , Volume 3, Issue 1, January 2013.

[11] Ankit Jairath, Puneet Namdeo ,"Low Power VLSI Techniques Using Booth Algorithm for Digital Filter for Hearing aid Applications" International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 2, February 2011 .

[12] Vasudev G. and Rajendra Hegadi," Design and Development of 8-Bits Fast Multiplier for LowPower Applications", Member, IACSITIACSIT International Journal of Engineering and Technology, Vol. 4, No. 6, December 2012.

[13] Lakhvinder Kaur, Parminder Singh Jassal," Synthesis And Simulation Of 8x8-Bit Modified Booth□s Multiplier", International Journal of Engineering Research & Technology (IJERT) Vol. 1 Issue 8, October - 2012.

[14] Young-Ho Seo, Dong-Wook Kim, “A New VLSI Architecture of Parallel Multiplier–Accumulator Based on Radix-2 Modified Booth Algorithm” IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 18, NO. 2, FEBRUARY 2010.

[15] Shaik.Kalisha Baba, D.Rajaramesh, "Design and Implementation of Advanced Modified Booth Encoding Multiplier", International Journal of Engineering Science Invention Volume 2 Issue 8 ,August. 2013 , PP.60-68.

[16] Kavita , Jasbir Kaur, "Design and Implementation of an Efficient Modified Booth Multiplier using VHDL", Special Issue: Proceedings of 2nd International Conference on Emerging Trends in Engineering and Management, ICETEM 2013.

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