An Efficient Power Saving Latch Based Flip-Flop Design for Low Power Applications

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ABSTRACT

In Integrated circuits a gargantuan portion of chip power is expended by clocking system which comprises of timing elements such as flip-flops, latches and clock distribution network. This paper enumerates power efficient design of shift registers using D flip-flops along with Clock and Power gating integration. In this paper we shown the Master-Slave design of D-Flip-Flop how we can reduce the number of transistors it the circuit. WE proposed a Latch based Flip-Flop which reduces the Master-Slave Network was shown. These circuits are designed and simulated using Tanner EDA Tools.
Keywords: Clock Gating (CG), Power Gating (PG).

1. INTRODUCTION

The tremendous advancements in VLSI technologies in the past few years have fuelled the need for intricate tradeoffs among speed, power dissipation and area. With gigahertz range microprocessors becoming common place along with the perennial increments in power dissipation, the emphasis is even more on pushing the speeds to their extreme while minimizing power dissipation and die area. The tremendous advancements in VLSI technologies in the past few years have fueled the need for intricate tradeoffs among speed, power dissipation and area. With gigahertz range microprocessors becoming common place along with the perennial increments in power dissipation, the emphasis is even more on pushing the speeds to their extreme while minimizing power dissipation and die area. The advancements has made speed area unit continually moving forward, from low scale integration to massive and VLSI and from MHz (MHz) to rate (GHz). The system necessities are rising up with this continuous advancing method of technology and speed of operation. In synchronous systems, high speed has been achieved exploitation advanced pipelining techniques. In fashionable deep-pipelined architectures, pushing the speed additional up demands a lower pipeline overhead. This overhead is that the latency related to the pipeline elements, like the flip-flops and latches.

Intensive work has been dedicated to improve the performance of the flip-flops within the past few decades. Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes. There are basically four main types of latches and flip-flops: SR, D, JK, and T, the major differences in these flip-flop types are the number of inputs they have and how they change state. For each type, there are also different variations that enhance their operations. D Flip-Flops are major contribution for design of any Digital Circuits. In this paper we shown the design of D Flip-Flop using Master-Slave network and how we can reduce the number of transistors in the Flip-Flop was shown in the below sections.

2. EXISTING SYSTEM

In existing system we were implemented conventional Flip-Flop. It has more power dissipation compare to proposed design.
2.1 Disadvantages:
- High power dissipation.
- More number of transistor.
- Reduce the power consumption.

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3.PROPOSED SYSTEM

In proposed system we will implement using Static Pass Transistor Logic (SPTL).

3.1DESIGN APPROACH

In order to reduce the power of the FF while keeping competitive performance and similar cell area, we tried to reduce the transistor count, especially those operating with clock signals, without introducing any dynamic or pre-charge circuit. The power of the FF is mostly dissipated in the operation of clock-related transistors, and reduction of transistor count is effective to avoid cell area increase and to reduce load capacitance in internal nodes. To reduce the transistor-count based on logical equivalence, we consider a method consisting of the following two steps. As the first step, we plan to have a circuit with two or more logically equivalent AND or OR logic parts which have the same input signal combination, especially including clock signal as the input signals. Then, merge those parts in transistor level as the second step.

3.2Proposed FF and Transistor Level Compression

After investigating many kinds of latch circuits, we have set up an unconventionally structured FF, shown in Fig. 7. This FF consists of different types of latches in the master and the slave parts. The slave-latch is a well-known Reset-Set (RS) type, but the master-latch is an asymmetrical single data input type. The feature of this circuit is that it operates in single phase clock, and it has two sets of logically equivalent input AND logic, X1 and Y1, and X2 and Y2. Fig. 8 shows the transistor-level schematic of Fig. 7. Based on this schematic, logically equivalent transistors are merged as follows. For the PMOS side, two transistor pairs in M1 and S1 blocks in Fig. 8 can be shared as shown in Fig. 9. When either N3 or CP is Low, the shared common node becomes VDD voltage level, and N2 and N5 nodes are controlled by PMOS transistors gated N1 and N4 individually. When both N3 and CP are High, both N2 and N5 nodes are pulled down to VSS by NMOS transistors gated N3 and CP. As well as M1 and S1 blocks, two PMOS transistor pairs in M2 This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.
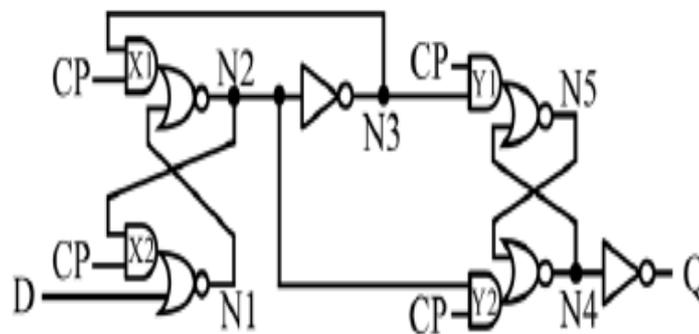

Fig1: Proposed Topologically Compressed Flip-Flop

This FF consists of different types of latches in the master and the slave parts. The slave-latch is a well-known Reset-Set (RS) type, but the master-latch is an asymmetrical single data-input type.

3.2.1 Approach of the Flip-Flop

- The feature of this circuit is that it operates in single phase clock, and it has two sets of logically equivalent input AND logic, X1 and Y1, and X2 and Y2 To reduce the transistor-count based on logical equivalence, we consider a method consisting of the following two steps

- As the first step, we plan to have a circuit with two or more logically equivalent AND or OR logic parts which have the same input signal combination, especially including clock signal as the input signals.

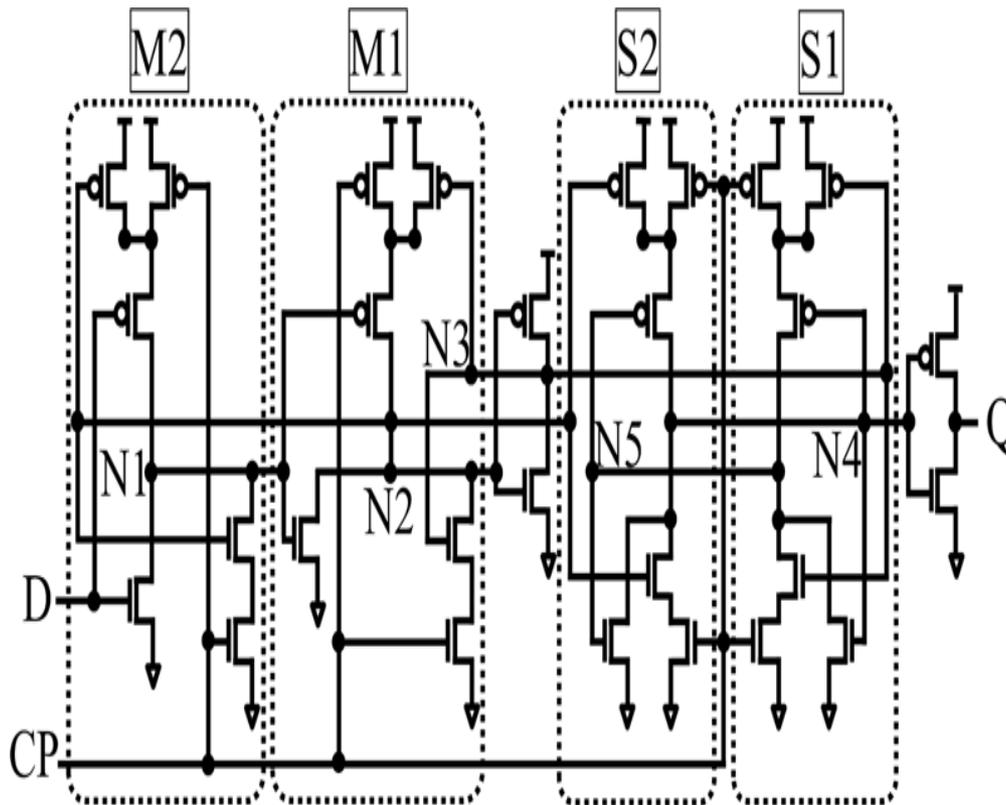- Then, merge those parts in transistor level as the second step

Fig2: Transistor Level Schematic

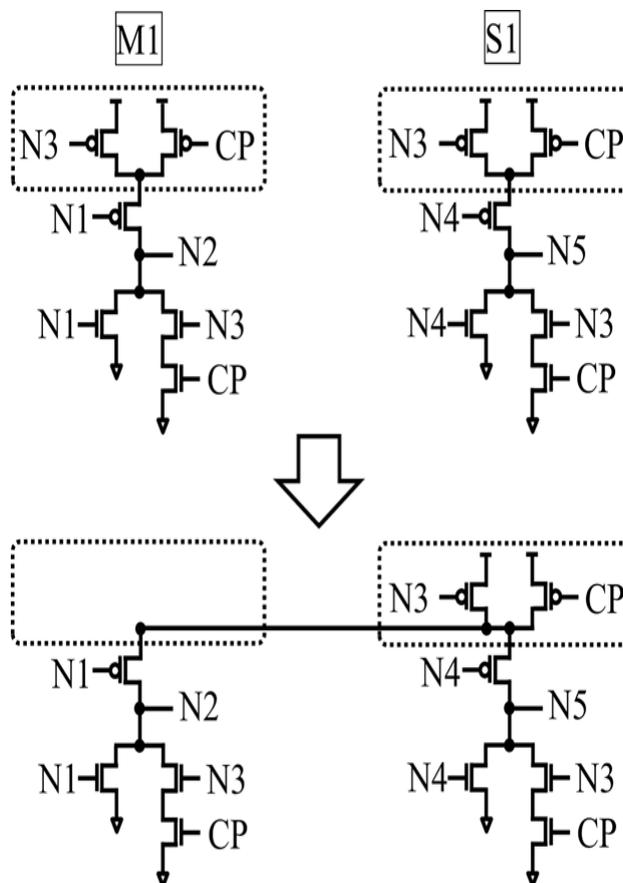Transistor merging at the PMOS side was shown in the below circuits are shown

Fig3: Transistor Merging at PMOS Side

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Transistor merging at the NMOS side was shown in the below circuits are shown
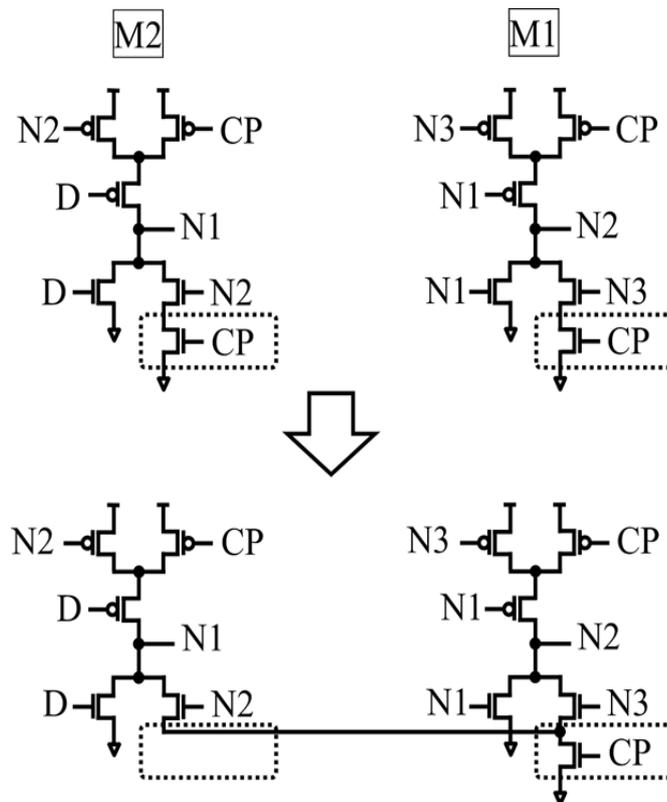
Fig4: Transistor Merging at NMOS Side

Fig5: Further Reduction at PMOS Side

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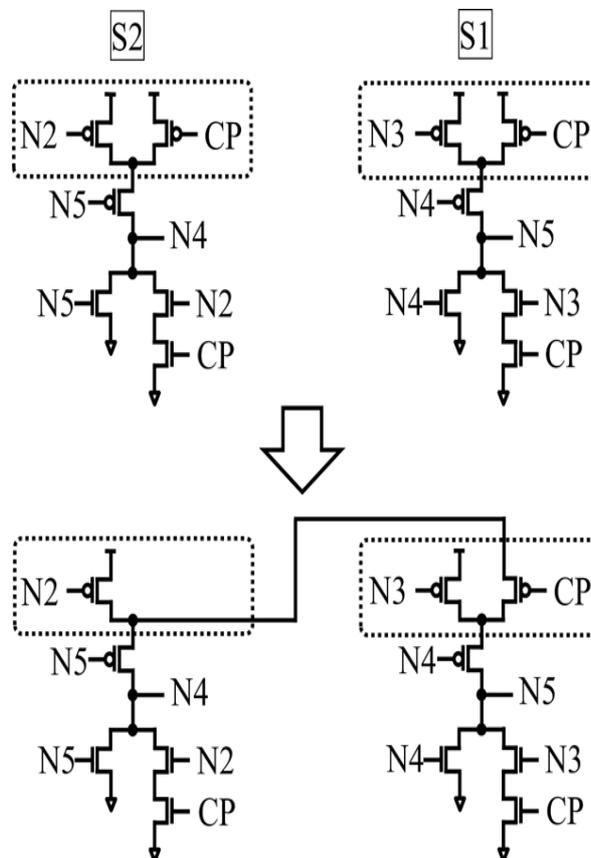**Volume 4, Issue 12, December 2015**   **ISSN 2319 - 4847**
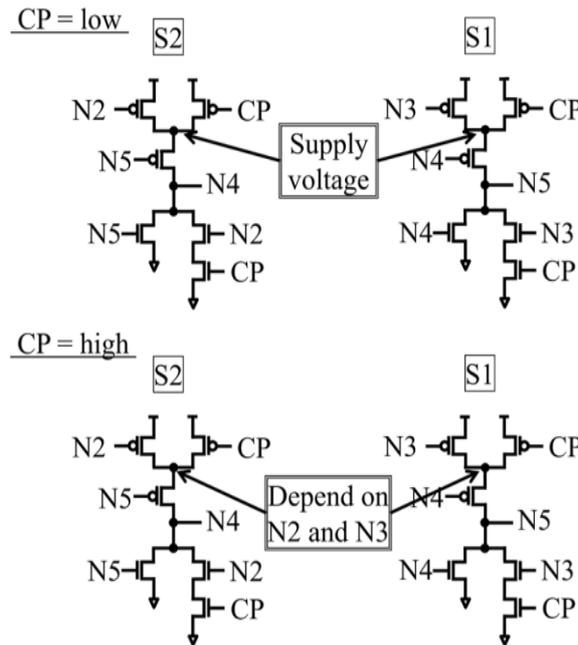
Fig6: The state of internal nodes

Further in the PMOS side, CP-input transistors in S1 and S2, shown in Fig. 11, can be merged, because N2 and N3 are logically inverted to each other. When CP is Low, both nodes are in VDD voltage level, and either N2 or N3 is ON. When CP is High, each node is in independent voltage level as shown in Fig. 12. In consideration of this behavior, the CP input transistors are shared and connected as shown in Fig. 11. The CP-input transistor is working as a switch to connect S1 and S2. This process leads to the circuit shown in Fig. 13. This circuit consists of seven fewer transistors than the original circuit shown in Fig. 8. The number of clock-related transistors is only three. Note that there is no dynamic circuit or pre-charge circuit, thus, no extra power dissipation emerges. We call this reduction.
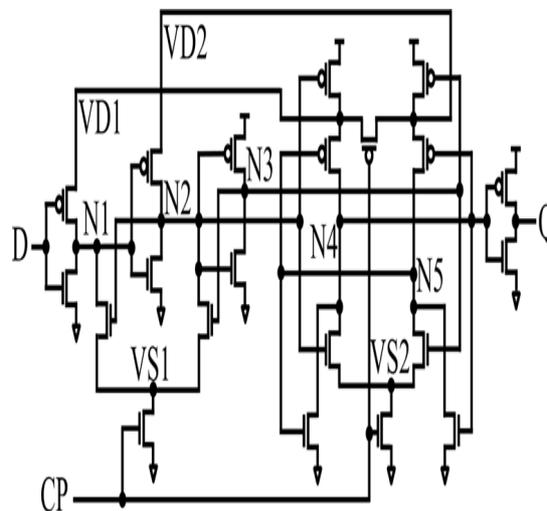

Fig7: Transistor level schematic of topologically-compressed flip-flop:

3.2.2 Cell Operation:
The Fig. 7 shows simulation waveforms of the circuit shown in Fig.6. In Fig. 6, when CP is low, the PMOS transistor connected to CP turns on and the master latch becomes the data input mode. Both VD1 and VD2 are pulled up to power-supply level, and the input data from D is stored in the master latch. When CP is high, the PMOS transistor connected to CP turns This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

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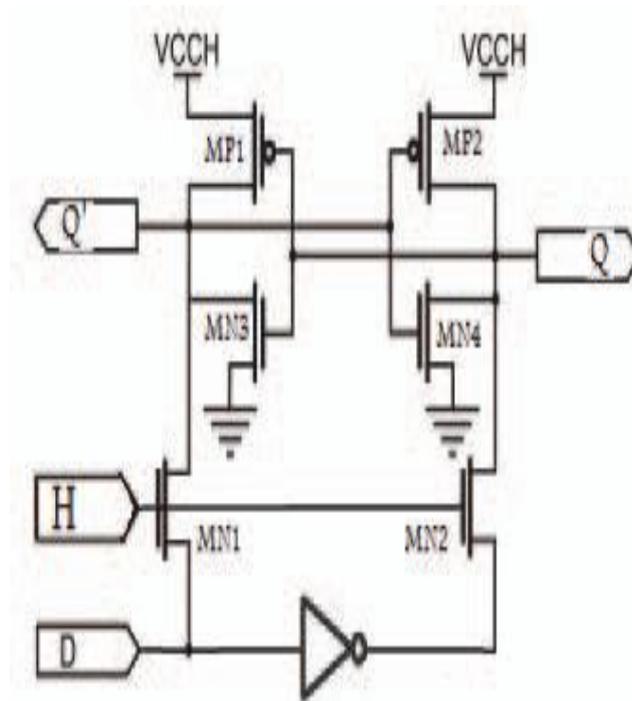
3.2.2   Schematic of Proposed Flip-Flop

Fig8: Proposed Flip-Flop

when the pulses are low in node H, MN1 and MN2 will be turned off, so it leads to a decrease in the leakage current in the off mode. During Clock is high the data was passed through the NMOS and Latching procedure starts MP1,MP2 and MN1,MN2.

4 Simulation Results

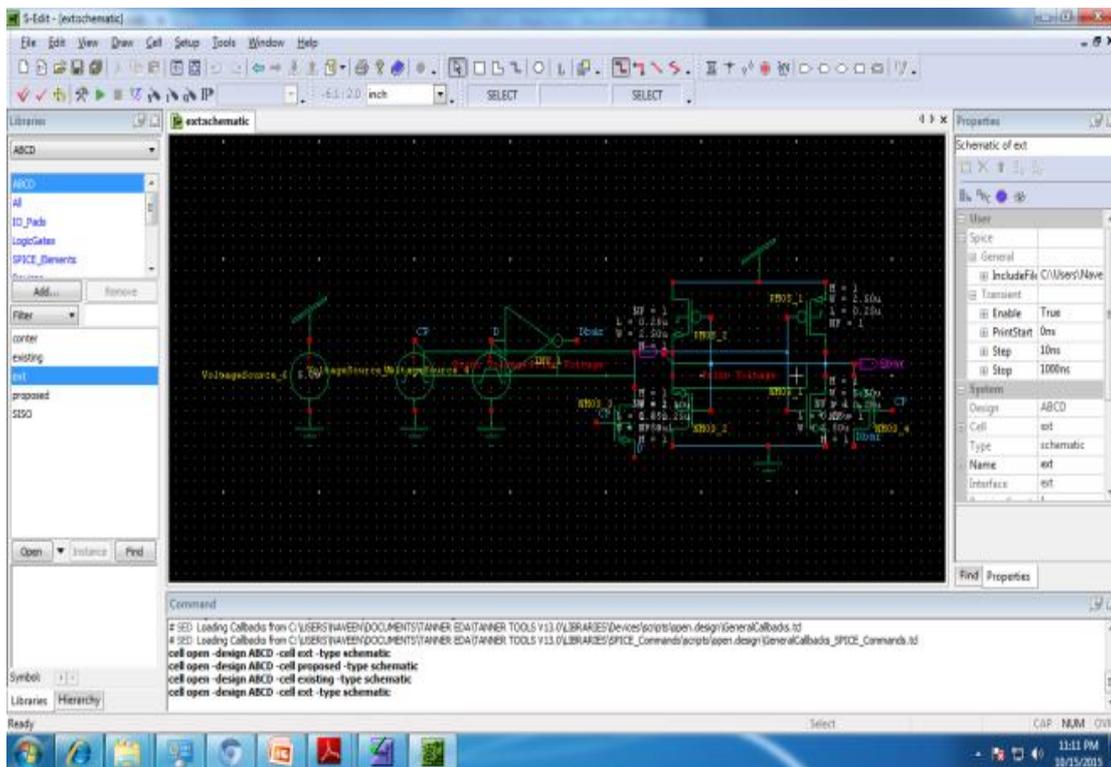These circuits are designed using S-Edit and Simulated using T-Spice simulation
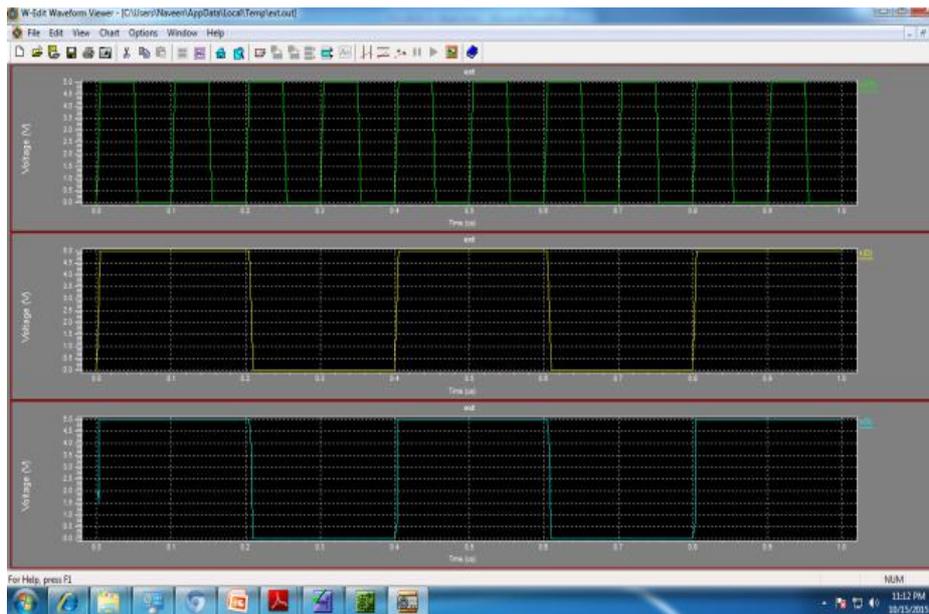

Fig 9: Design of Proposed Flip-Flop

Fig10: Simulation of Proposed Flip-Flop

4.1.1 Tabulation

Table 1: In the tabulation we show the power comparisons of the Flip-Flops

Circuit	Power Dissipation
Existing Flip-Flop	8.967205e-004 watts
Proposed Flip-Flop	1.138522e-004 watts
Latch Based Flip-FLop	2.951426e-008 watts

5. CONCLUSION

An extremely low-power FF was shown in this paper which reduces the number of transistors for the Flip-Flop design as well as it reduces the power consumption as shown in the above table.

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AUTHOR

N Kiran received his B.Tech in Electronics and Communication Engineering from ABR College of Engineering and Technology, KANIGIRI in 2012 and currently pursuing his M Tech in VLSI & ES in VRS & YRN College of Engineering and Technology, Chirala and his research interest in Low Power VLSI Designing.