FPGA-Based Implementation of IEEE 802.16d WiMAX Baseband system

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ABSTRACT

The current communication systems tend to use wireless broadband access technologies that provide many features to its subscribers, such as high speed data connectivity and good voice quality and video services for economical rates. WiMAX is one of the wireless broadband technologies, based on the standard IEEE 802.16 wireless metropolitan area network. The physical layer of WiMAX based on OFDM technique, in order to provide high data rates, minimize inter-symbol interference and fading effect. The designed system includes a data randomized module, error detection and correction module, mapping module that aid transmit more bits/symbol, pilot insertion and guard interval for estimation and reduce ISI, 256-point IFFT to generate OFDM symbols, long preamble for timing synchronization, and 64 cyclic prefix addition to combat the effect of fading channels. The complementary operations apply to the receiver blocks in reverse order. This paper presents a model for simulating and implementation of a complete WiMAX baseband system. First, the simulation was done using a Xilinx system generator incorporated with Simulink/Matlab and then it synthesized, implemented and verified as digital hardware using VHDL language and Xilinx ISE design suite with Spartan 3E XC320S1200 FPGA.

Keywords: WiMAX, Physical Layer, OFDM, FPGA

1. INTRODUCTION

The explosive growth of the internet over the last decade has lead to an increasing demand for high speedinternet access. Worldwide introprobability for microwave access (WiMAX) is a broadband wireless access (BWA) based on wireless metropolitan area networking (WMAN) standards developed by the IEEE 802.16 group has increasingly gained popularity as an alternative “last mile” technology to digital subscriber line (DSL) and cable modems. It has been proposed as a promising wireless communication technology due to the fact that it can provide high data rate communications in MAN [1]. Following the hugely successful global deployment of the 802.11 wireless local area network (WLAN) standard. WiMAX supports a maximum range of approximately 50Km for single hop architecture in the presence of line of sight (LOS) and 25Km in non-line of sight (NLOS) connectivity. The physical layer of WiMAX based on orthogonal frequency division multiplexing (OFDM), which had become very popular in these days, allowing high speed of wireless communications [2]. OFDM technique is widely adopted in this system due to its robustness against multipath fading and simpler equalization scheme [3]. IEEE 802.16d standard defines two preambles structure to work out the synchronization problem [1]. One is the long preamble and it is applicable to network in the downlink; the other is short preamble and it is applicable to network in the uplink. The first symbol consists of four repetitions of 64 sample fragment preceded by cyclic prefix (CP), the second symbol consists of two repetitions of 128 sample fragment preceded by a CP in the time domain. In this paper, we interested on symbol synchronization algorithm about the network in the downlink, so it mainly refers to long preamble.Since WiMAX baseband physical layer carried out in the digital domain, several methods used to implement the system. One of the ways by using a general purpose microprocessor (µP), digital signal processing is an example of µP that performs complex algorithm, which are used for a wide range of applications, from communications and controls to speech processing [4]. The disadvantage of using this hardware are: needs a peripheral chips and memory to support the operation, required high power, and slowest in terms of time to produce the output. Other methods to implement the system are application specific integrated circuit (ASIC) and field programmable gate array (FPGA), ASIC offer the ultimate in size (the number of transistors), complexity, and performance; designing and building one is an extremely time-consuming and expensive process, with the added disadvantage that the final design is “frozen in silicon” and cannot be modified without creating a new version of the device. Unlike the ASIC, FPGA can be reprogrammed multiple times, thus Implementation design changes is much easier in FPGA. The time-to-market for such designs are much faster and the cost of an FPGA design is much lower than that of an ASIC[5]. The architecture of a typical FPGA is shown in figure 1. It is array of multiple configuration logic blocks (CLBs), input –output blocks (IOBs), and a sea of interconnect blocks. The interconnect connects CLBs together so that more complicate circuits can be composed from primitive logic gates. The bit stream file specifies the configuration of both CLBs and the interconnect blocks. Lookup table (LUT) uses static random access memory (SRAM) cells as programming bits and can implement any N- input function [6].

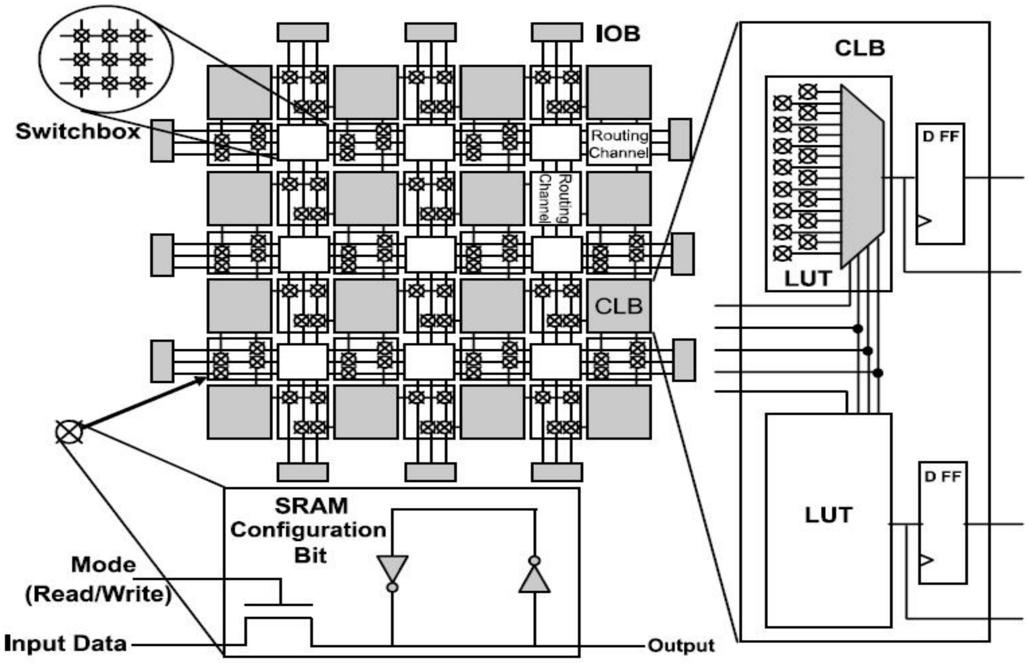

Figure 1: FPGA architecture [6].

In recent years a number tools such as system generator environment from Xilinx, has been developed which facilitate the design of algorithms for DSP on FPGA [7] . System Generator is a system-level modeling tool that facilitates the FPGA hardware design. It extends Simulink in many ways to provide a modeling environment that is well suited to hardware design. The tool provides high-level abstractions that are automatically compiled into an FPGA at the push of a button. The tool also provides access to underlying FPGA resources through low-level abstractions, allowing the construction of highly efficient FPGA designs [8]. In this paper, an introduction to WiMAX and hardware implementation are presented in section (1). Section (2) presents a brief description of related work. Then section (3) and (4) describes respectively, Block diagram of WiMAX -based OFDM Physical Layer and simulation results, finally section (5) present conclusions and future work.

2. RELATED WORK

There are a number of papers [9-17] related to OFDM implementation for IEEE 802.11 and IEEE 802.16. But most of them are simply parts of a baseband system like a transmitter without coding and a receiver without packet detection, channel estimation, equalization and decoding. Manavi and Shayan [9], have implemented an uncoded OFDM system on Xilinx Virtex-II FPGA chip based on IEEE 802.11a. The implemented transmitter included a symbol mapper (BPSK, QPSK, 16QAM and 64QAM), IFFT and cyclic extension blocks. The implemented receiver consists of the guard time removal, FFT, symbol demapper. The system included a synchronization circuitry used for packet detection and time synchronization. Kadiran [10], has implemented single modulation OFDM system with 8-point FFT processor on Apex 20KE FPGA board. The design included mapping block (BPSK), s/p and p/s block set and 8-point FFT processor. The implemented system lacked accuracy in the generated OFDM signal since; an 8-bit resolution bus was used to represent the OFDM signal. Veilleux, etal. [11], have implemented an uncoded Adaptive OFDM system with 4 modulation schemes BPSK, 4QAM (or QPSK) and 16QAM using channel estimator Frequency Pilot Time Average (FPTA-2). The designed system has been implemented on one high-end FPGA chip. Shahid [12], has implemented of OFDM transmitter compliant IEEE 802.16d on Altera cyclone IIEP2C 35F672C6 FPGA using Quartus II 9.0 Software, with error correction encoder and four modulation types (BPSK, QPSK, 16 QAM, 64 QAM). But without Receiver module. Brannstrom [13], has implemented an OFDM transmitter on Altera Statix II FPGA based on IEEE 802.11a. The design software used was Quartus II from Altera and ModelSim and Precision RTL Synthesis from Mentor Graphics. Serra [14], shows the design of an OFDM transmitter as a part of an OFDM demonstrator Hiperlan 2 for the following specifications: ¾ punctured code rate, 16QAM, 64-IFFT and cyclic prefix of16 samples. Mohamed [15], has implemented OFDM physical layer. Firstly, using Matlab program to see the simulation results for three experiments, each one has varying FFT point and SNR, after that implemented on Xilinx Spartan 3AKit without coding. Cheng [16], has proposed an OFDM system with 8-point FFT processor design by using VHDL, simulated using Altera Max Plus II. The work focuses on 8 point Fast Fourier Transform (FFT) for receiver and transmitter part. Nasreen [17], Implemented OFDM transmitter and receiver using the Quartus II tool and simulation have been carried out using Altera modelsim simulation with 64 FFT, 8 CP QPSK constellation mapper.In this paper, a discussion of the WiMAX -based OFDM baseband system in pipeline architecture based on IEEE 802.16d protocol will be presented. Also algorithms are realized on FPGA platform, including randomization, coding, different types of modulation, 256-point FFT, channel estimation, equalization, packet detection, and a control units. This project passes loop-mode test in Xilinx Spartan 3E XC320S1200 FPGA.

3. Block diagram of WiMAX-based OFDM Physical Layer

WiMAX technology is a broadband wireless network in MAN based on IEEE 802.16. The IEEE 802.16 working group was formed in July 1999, the first version was approved in December 2001 for the high frequency range, a modification is done in 2004 to support fixed applications while the mobile application presented in 2005. Table I, shows a comparison of these versions [18][1][19]. The physical layer is responsible for the physical connections, functionsthat are required (type of modulation, coding, binary transmission rate) to transport data bits between the physical ends of the communication link.

Table I: Basic Data of IEEE 802.16 [18][1][19

a)	b)IEEE 802.16-2001	c) IEEE 802.16d-2004	d)IEEE 802.16e-2005
Completed	December 2001	June 2004	December 2005
Spectrum	10-66GHz	<11GHz	<6GHz
Propagation	LOS	NLOS	NLOS
Modulation	QPSK,16QAM 64QAM	256 subcarriers OFDM, QPSK,16QAM, 64QAM	OFDMA,QPSK, 16QAM,64QAM 256QAM
Mobility	Fixed system	Fixed system	Mobile system

An implementation of Wireless MAN-OFDM physical layer (Transmitter and Receiver) of IEEE 802.16d standard are presented in figure2and figure 3, respectively, using Simulink and System Generator. This physical layer uses 256 subcarriers, which are assigned as follows: 192 for data subcarriers, 56 used as null guard bands, 28 and 27 at the beginning and at the end respectively, a central one as a DC frequency, and 8 pilot subcarriers. The block system is divided into three main sections: transmitter, receiver and channel.

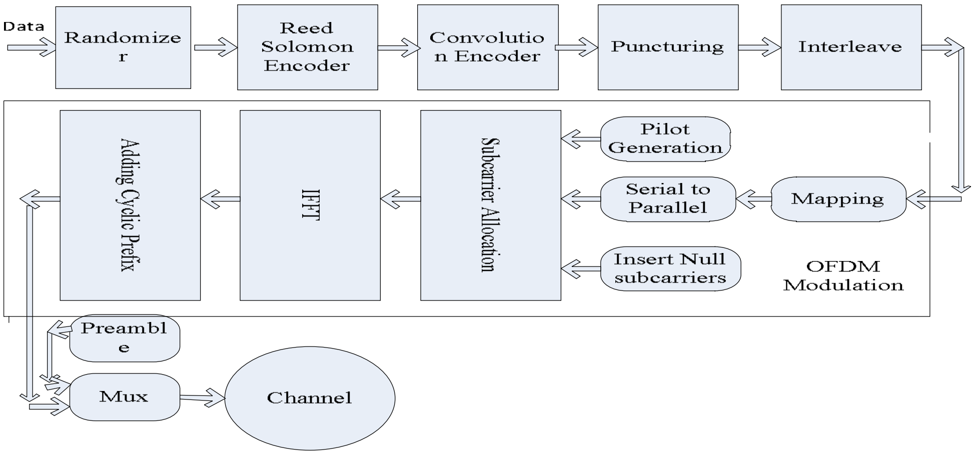

Figure 2: IEEE 802.16d Transmitter Architecture [1]

3.1 Randomizer/ De-Randomizer

A Randomizer is a device that transposes or encodes a message to make it unintelligible at the receiver that not equipped with an appropriately set de-Randomizer device.The Pseudo- Random Binary Sequence Generator (PRBS) used for randomization, and shown in figure 4. Read only memory, used to store a pre-calculated PRBS, but in this paper it is generated by a linear feedback shift register (LFSR). The de-Randomizer has been just the same device as the Randomizer, which defined by the polynomial of its LFSR ($1 + X^{4} + X^{6}$) with initial state of ones.

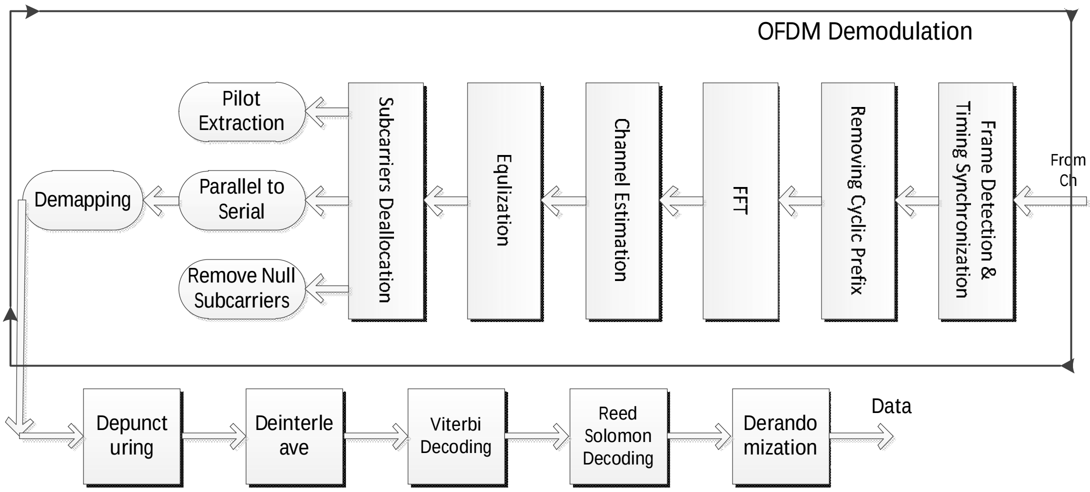

Figure 3: IEEE 802.16d Receiver Architecture.

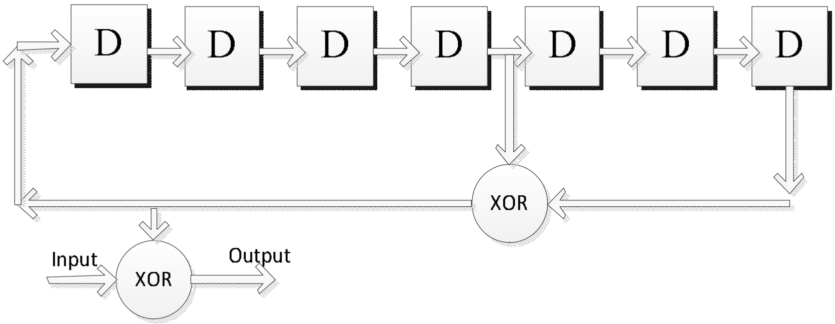

Figure 4 : Randomizer / De-Randomizer [1]

3.2 Reed Solomon Encoder / Decoder

The Reed Solomon encoder (RS) operates in the following way: the encoder takes k bytes of information and adds parity bytes to obtain a code word of n bytes. A decoder can correct up to t erroneous bytes per code word, where t = ((n-k)) / 2. A RS code and its variables n, k and t can be written as a vectorin the following way: RS (11, 15, 4). This indicates an RS code with a code word n = 15 bytes, k = 11 bytes of information, and can correct up to t = 2 bytes of error as shown in figure5

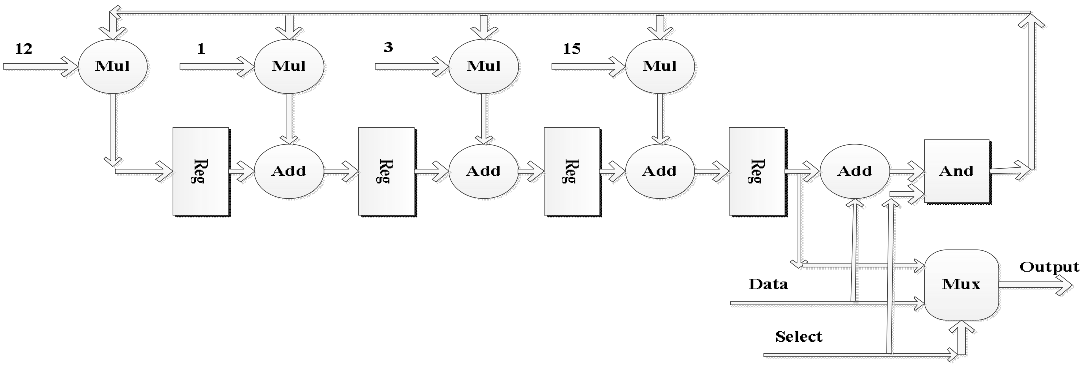

Figure 5: Reed Solomon Encoder

3.3 Convolution Encoder / Viterbi Decoder

After Rees Solomon encoding process, data bits are further encoded by convolutional code that is an error correcting code that processes information serially. it has a memory that the output symbols depend not only on the input symbols, but also on previous inputs and/or outputs. Viterbi Decoding Algorithm is used for decoding convolutional codes.This algorithm was introduced by A. J. Viterbi in 1967. Figure 6, shows the representation of a ½ rate convolutional encoder with generator polynomials G1 = 133oct to output X, and G2 = 171oct to output Y.

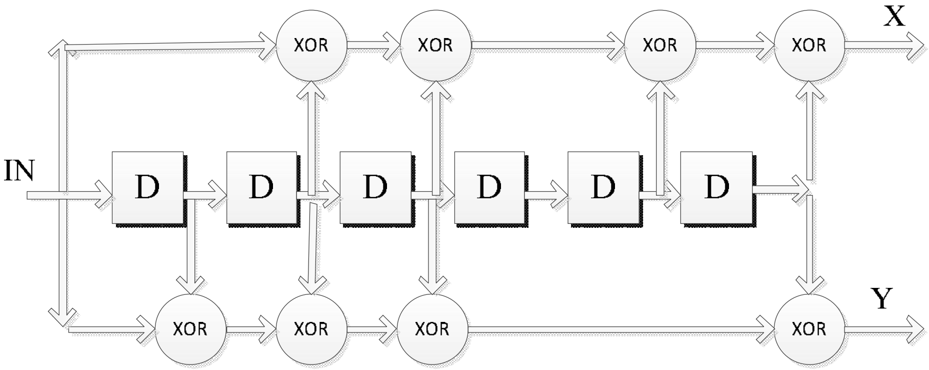

Figure 6: Convolutional Encoder with ½ rate [1]

3.4 Puncturing / De-puncturing

Some of the parity bits are removed after coding; this process is known as puncturing. The puncturing pattern serves for adjusting the rate of transport channels to the available bit rate in physical channels. At receiver, zeroes were insertedfor de-puncturing. Figure 7, shows the puncturing.

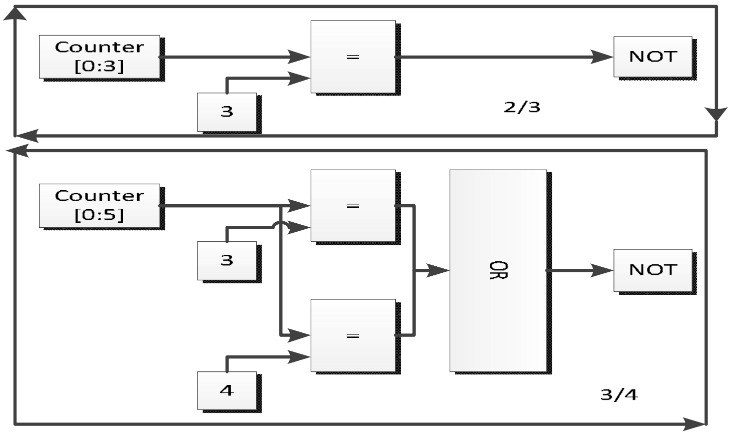

Figure 7: Puncture with different code rate 2/3 and ¾

3.5 Interleaver / De-Interleaver

Interleaving technique is used for improving the performance of error correcting codes. The interleave consist of two permutation steps, the first permutation step is the adjacent coded bits are assigned to non-adjacent subcarriers. By the second permutation step, the bit index of the consecutive coded bits onto the constellation is changing continuously. figure 8, shows the interleave process,the index of the data was represented by ROM

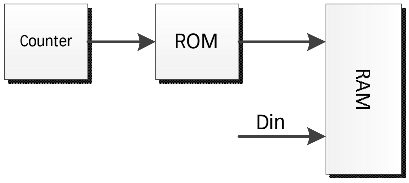

Figure 8: Interleaver process with a memory

3.6 Mapping

The mapper converts input data into complex valued constellation points,according to a given constellation: QPSK, 16QAM, or 64QAM as shown in figure 9. The amount of data transmitted on each subcarrier depends on the constellation, like QPSK and 16QAM transmit two and four data bits per subcarrier, respectively. Which constellation to use depends on the channel quality. On a channel with high interference a small constellation like QPSK is favorable, since the required signal to noise ratio (SNR) in the receiver is low, whereas in interference free channel a larger constellation is more beneficial due to the higher bit rate

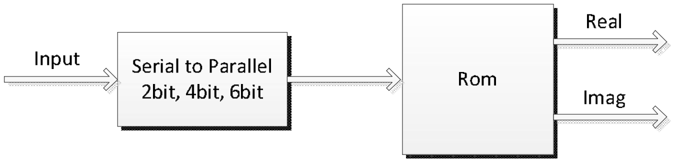

Figure 9: Mapping with 2, 4, and 6bits/symbol

3.7 Inverse Fast Fourier Transform (IFFT)

The real and imag parts, each of 192 data subcarriers are fed into IFFT symbol assembler which inserts pilot, DC and guard carriers to make a total of 256 carriers for OFDM realization. This work uses a radix-2 butterfly generated by the Xilinx IP core Generator. The IFFT is used for converting the data on frequency domain into the time domain. It is used to generate OFDM symbols. IFFT is defined by the equation [10]

$$x(n) = \frac{1}{N}\sum_{k=0}^{N-1} X(K)\,W^{-nk}, k = 0,1,\ldots N-1$$

(1)

The cyclic Prefix (CP) is added, which is a copy of the last N samples from the IFFT that are placed at the beginning of the OFDM frame to overcome ISI problem. It is important to choose the minimum necessary CP to maximize the efficiency of the system.

3.8 Wireless Channel

The transmission medium faces many problems, in wireless communication environments, signals may encounter, reflection, refraction, and scattering during its propagation. Therefore, they arrive at the receiver through many different paths. This phenomenon is called multipath transmission, thus the received signal has attenuation with a number of delays.

3.9 Timing Synchronization

A misalignment between the sent symbol and the demodulated symbol can introduce ISI (timing error). This error can deteriorate modulation performance. To face this problem, a long preamble structure will be used. The autocorrelation will be used for frame synchronization [20]. The auto correlation relies on product between the conjugate of samples from the first half and the corresponding samples from the second half, so that the products of each of these pairs of samples will have approximately the same phase and hence the magnitude of the sum will be peaked. If L is the number of complex samples in one half of long preamble which is 128 samples, then P(n) and R(n) are calculated as

$$P(n) = \sum_{m=0}^{L-1} y^{*}(n+m)\,y(n+m+L)$$

(2)

$$R(n) = \sum_{m=0}^{L-1} |y(n+m+L)|^{2}$$

(3)

Where P(n) is the sum of the pairs of products, R(n) is the received energy for the second half of long preamble, y is the received signal, n is the timing index, and the timing metric is

$$M1(n) = \frac{|P(n)|^{2}}{(R(n))^{2}} \quad (4)$$

Figure 10, shows the timing metric for free noise, where the plateau is clearly obvious and completely flat, this is the ideal state of synchronizer in which any point within the plateau can be chosen to start the data symbol. It can be seen from figure 10, the plateau is not obtained due to noise variation for very low SNR .

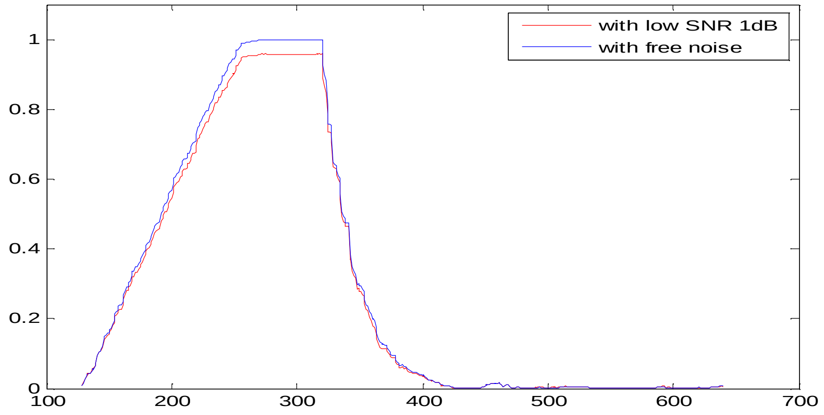

Figure 10: Timing metric M1(n) for auto correlation for 1 frame.

Figure 11, shows the block diagram of synchronization, in which D = 128.

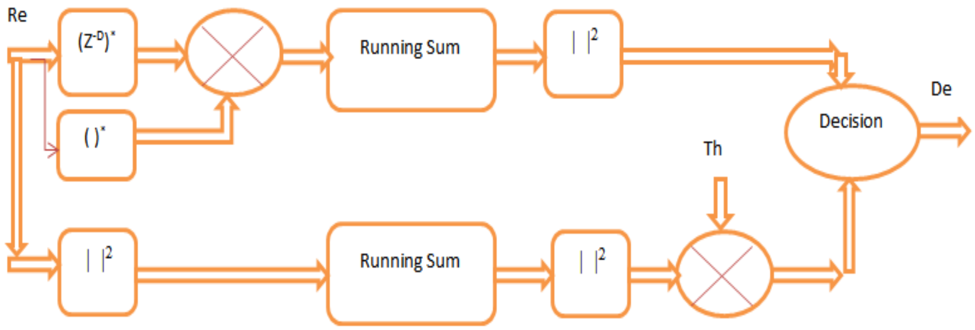

Figure 11: Block diagram for synchronization [20]

3.10 Channel Estimation

The received signal is usually distorted by the channel environment. In order to recover the transmitted bits, the channel effect must be estimated and compensated within the receiver [21]. A training symbols are one method to find channel frequency response (CFR) and it is must be known to both transmitter and receiver.

3.11 Equalizer

To restore the transmitted signal, a simple equalizer is used, that applies the inverse of the channel frequency response (CFR) that was estimated. Figure 12, illustrate a flat frequency response by combination the channel and equalizer output response [22].Figure 13, shows the channel estimation and equalization.

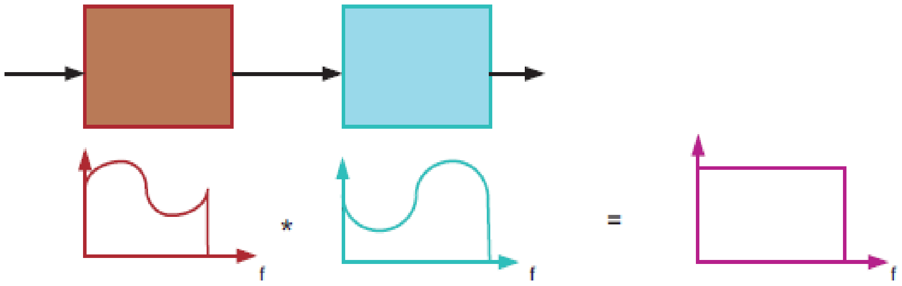

Figure 12: Equalizer

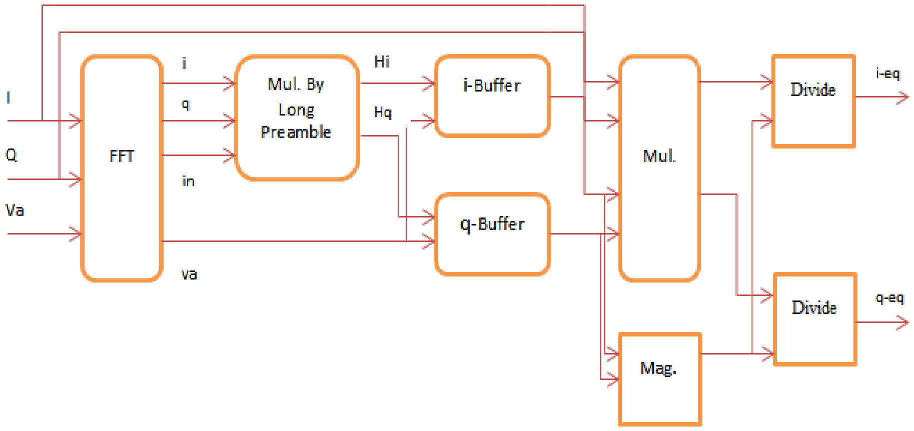

Figure 13: Channel estimation and equalization.

4. Simulation Results

The complete WiMAX baseband system comprising of the transmitter and the receiver, has been implemented on a single FPGA board (Xilinx Spartan -3E XC3S1200E). The software used is the Simulink/Matlab 7.14.0.739 (R2012a) incorporated with Xilinx system generator and Xilinx ISE (Integrated Synthesis Environment) design suite v14.5. The VHDL language used as the hardware description language (HDL).The development process for the system that shown in figures (2,3), is shown in figure 14, where Xilinx block-sets change the floating-point algorithm to fixed-point logic. Xilinx core generator represents an optimization for hardware resources. The system generator automatically integrates for FPGA andthe system defined parameters will be corresponded to the hardware and input and output ports, so it will automatically complete synthesis, simulation, and implementation.

The physical layer parameters are

- OFDM with 256 subcarriers includes 192 data, 8 pilots, and 56 guardband.
- All subcarriers were modulated using QPSK, 16 QAM, 64 QAM.
- 256-point IFFT.
- Randomization with 7 shift register.
- Forward error Correction: Reed Solomon code (11,15,2) and Convolutional code (m=1, n=2, constraint length k=7) with rate ½ .
- Interleave plus Puncture (2/3 and 3/4) code rate.
- 64- Cyclic Prefix.
- Long Preamble (64+128+128).
- Data detection using auto correlation method.
- Equalization and Channel Estimation using long Preamble.
- OFDM symbol =Tifft +Tg

$$\text{Tifft} = \frac{1}{\Delta f} = \frac{256}{20} = 12.8\mu s \quad \text{for } 20 \text{ MI}$$

$$\text{Tg} = \frac{12.8}{4} = 3.2$$

$$\text{OFDM symbol} = 16$$

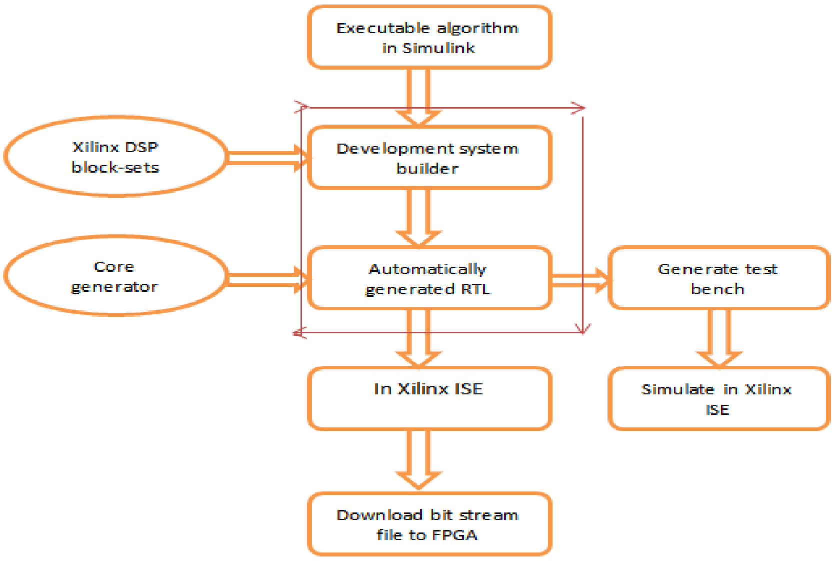
Executable algorithm in Simulink
Xilinx DSP block-sets
Development system builder
Core generator
Automatically generated RTL
Generate test bench
In Xilinx ISE
Simulate in Xilinx ISE
Download bit stream file to FPGA

Figure 14: System development process

Figure 15, shows the input and output of data randomized, the data input is sent to Randomizer, where data are randomized to avoid long sequence of 0's and 1's. Figure 16, shows the input and output of forward error correction (Reed Solomon Encoder and Convolutional Encoder), the randomized output is sent to the FEC, its add redundant bits to the message. The redundancy allows the receiver to detect and correct a limited number of errors occurring anywhere in the message. The output of FEC is fed to puncture and interleave block to avoid long runs of low reliable bits as shown in figure 17. The input and output of the modulation scheme (QPSK), data allocation (Guard band , Data, and Pilots) also shown in figure 17. The subcarrier indices are protocol- specific. The IFFT convert the frequency domain to time domain as shown in figure 18, the size of the IFFT is determined by the number of subcarriers that is 256-point of this paper. 64-cyclic prefix from the end 256-subcarriers and added to the beginning, thoseshown in figure 18, the purpose of the cyclic prefix is to avoid inter-symbol interference caused by the multipath propagation. The preamble is shown in figure 19, which is known by the receiver so that it can detect the start of new transmission . Figure 20, shows the packet detection and figure 21, shows the FFT that converts the time domain to the frequency domain, channel estimation and equalization. The demodulated data for QPSK is shown in figure 22, it can be seen that the modulated data in figure 17and the demodulated in figure 22, are the same.Figure 23, shows the results obtained using the Xilinx ISE design suite, it's the same as shown in the other figures.The high precision implementation of the transceiver utilizes 11355 slices, 14942 flip-flops, 16 block RAMs, and 39 multipliers.

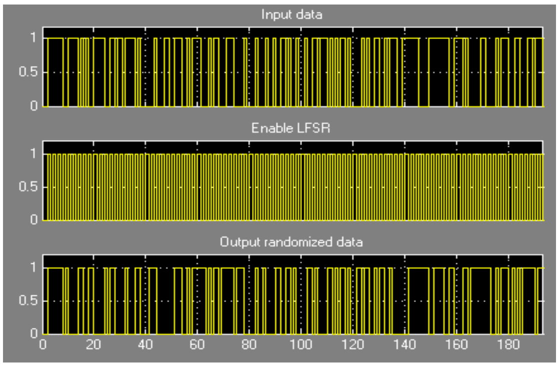

Figure 15: Input and output of data randomized

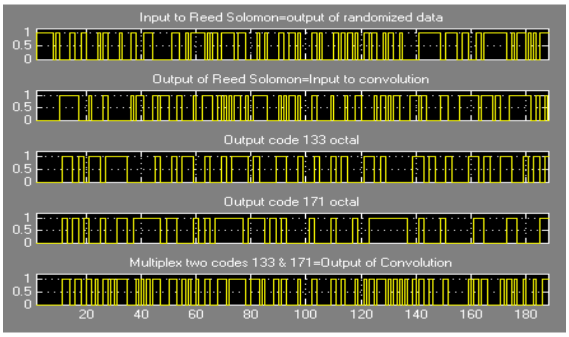

Figure 16: Input and output of forward error correction

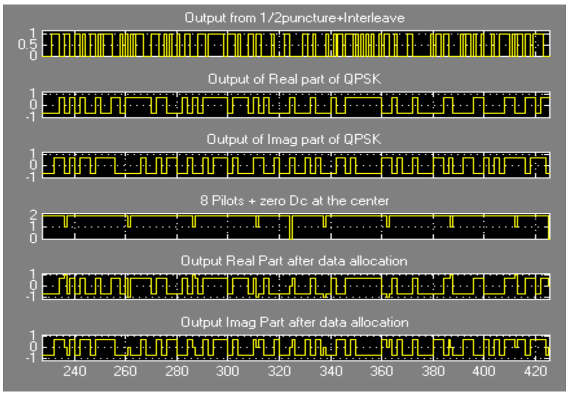

Figure 17 : Interleave, QPSK, and data allocation.

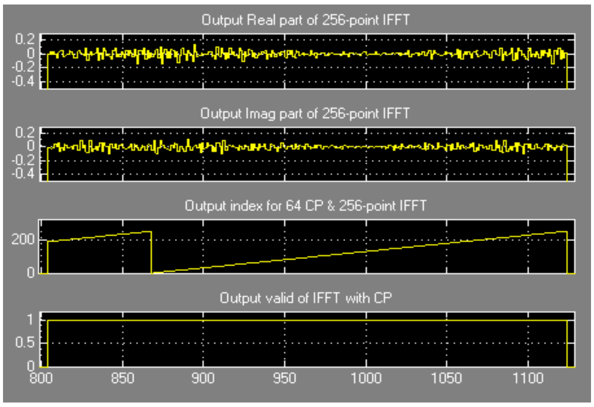

Figure 18 : 320 Samples include 256-IFFT and 64-CP.

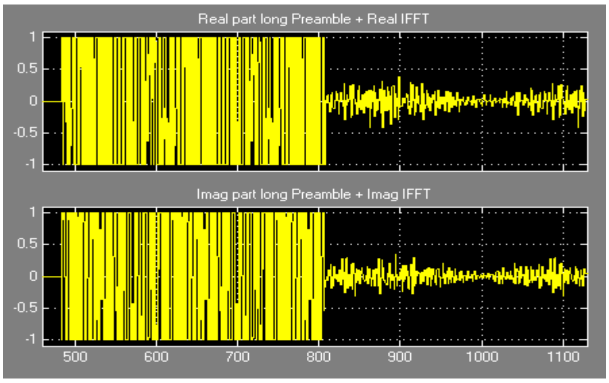

Figure 19: long preambles with data.**Figure 20** Data detection.

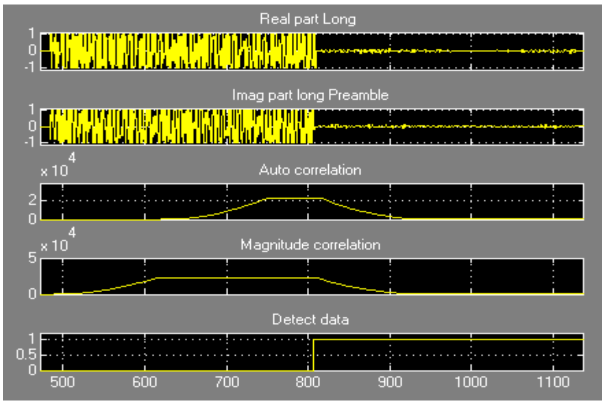

Figure 20: Data detection.

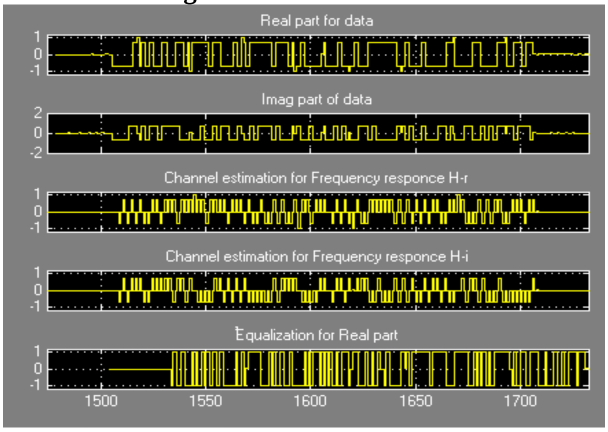

Figure 21: Output of FFT, Estimation, and Equalization.

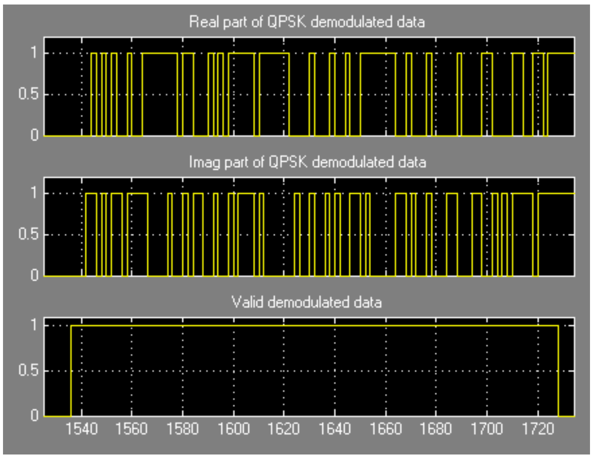

Figure 22: Demodulated data for QPSK.

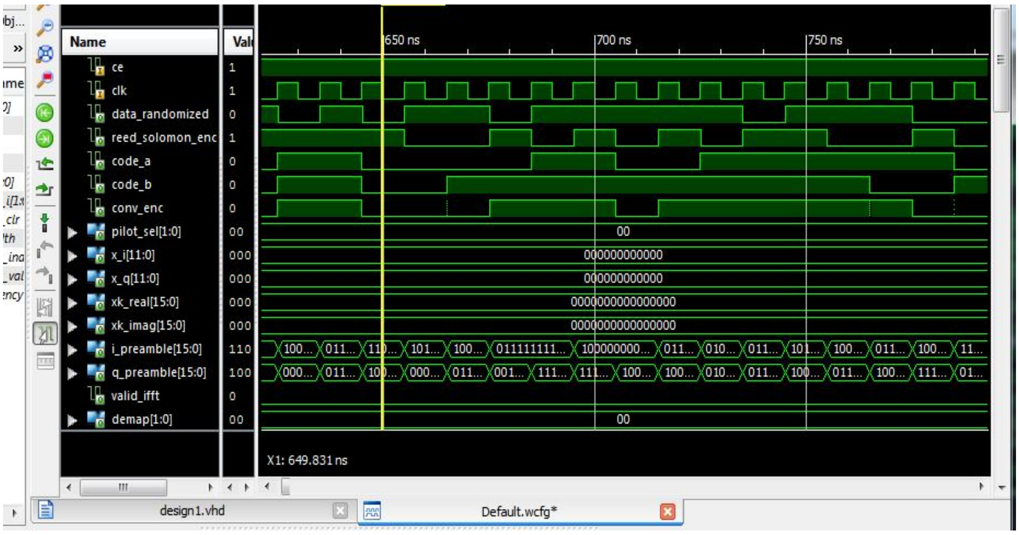

Figure 23: Results using Xilinx ise.

5.CONCLUSION AND FUTURE WORK

WiMAX is one of the most promising technology from among the existingtechnologies due to its unique features. OFDM used to implement the physical layer of the IEEE 802.16d wireless MAN standard. The overall IEEE 802.16d system has been modeled and simulated with basic blocks of Xilinx system generator for Simulink. This implementation environment enables development of high performance DSP systems and provides automatic hardware description language code generation. According to the simulations, the transmitter and the receiver have been developed in such a way that it is reliable and easy implemented. As a future work, the improvement in data transmission and resistance to fading channel, requires an advanced coding techniques, but this is out of the standard, the accuracy of channel estimation and equalization can be improved to be an adaptive channel estimation and equalization, also multi-input multi-output (MIMO) technology makes the system more reliable.

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