

Improved Stability SRAM Design for Low power Applications

Sai Silpa.Chandavolu¹, Prof. K. Amarnath²

¹ P.G Student, VRS&YRN College of Engineering & Technology, Vadaravuroad, Chirala

² Professor, VRS&YRN College of Engineering & Technology, Vadaravuroad, Chirala.

ABSTRACT

In this paper we modified the Schmitt Trigger based SRAM for the purpose of reduced power & area than the existing type of designs as well as the new design which is combined of virtual grounding with read Error Reduction Logic is compared with the existing technologies & the nanometer technology is also improved for the purpose of much improved reduction of area & power factors than the Schmitt Trigger based SRAM Designs the simulations were done using Tanner Tools.

Keywords: Static Random Access Memory (SRAM), Virtual Grounding, Error Reduction Logic, Schmitt Trigger SRAM, Tanner Tools.

1. INTRODUCTION

Aggressive scaling of semiconductor dimensions with every technology generation has resulted in raised integration density and improved device performance [1]. Leakage current will increase with the scaling of the device dimensions. Raised integration density at the side of raised outflow requirements ultralow-power operation was major one for operating a device. The ability demand for the battery-operated devices like cell phones and laptops is even additional tight. Reducing supply voltage reduces the dynamic power quadratic ally and leakage power linearly to the primary order. Hence, offer voltage scaling has remained the main focus of low power style. On chip caches plays a important in speed of Processors in order to increase the speed majorly now we increases the frequency of operation which makes caches to operate more faster . To achieve higher reliability longer battery life we require low power caches.

The Problem Found in the existing SRAM designs are listed below:

- SRAMs are consuming most of the power of the core Processor Element.
- The leakage in the SRAM circuit is high when compared to the all other processor components.
- As its consuming much power heat dissipation also occurs
- So less efficient than all other elements.

The total effect of the supply voltage scaling along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, write failure, and access-time failure

2. GENERAL SRAM

2.1 Conventional 6T SRAM design

There are many topologies for SRAM in past decades 6T SRAM got its attention for the tolerance capability for noise over another SRAM cell design. The 6T SRAM cell design [2]. The 6T SRAM cell design consists of two access transistors and two cross coupled CMOS inverters. Bit lines are the input/output ports of the cell with high capacitive loading. The operations READ and WRITE are conducted by these bit lines only, we will see how these are carried out.

2.1(a) Read Operation

Before starting of the read operation, we should charge the bit lines to VDD. When the word line (WL) is enabled, the bit line which connected to the node of the cell containing '0' is discharged through the NMOS transistor. By this we can know which node is containing '0' and which is having '1' in it. Using sense amplifiers we can know the node containing 1/0 by sensing the bit lines. The bit line containing '1' means it's connected to the node containing '1' and vice versa.

2.1(b) Write Operation

For writing 1/0 we should provide the data to the bit line (BL), with respect to the bit line bar (\overline{BL}). When the word line (WL) is enabled the data is written into respective node[3][4][5].

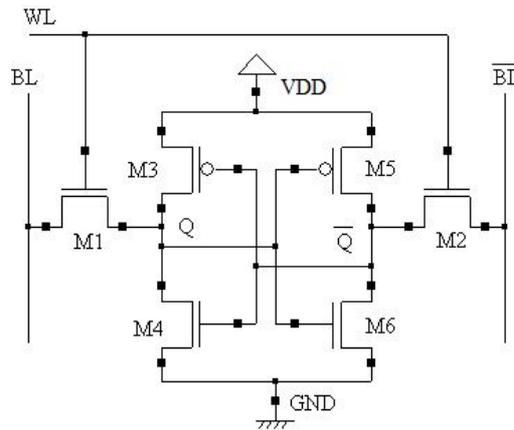


Figure 1: Conventional 6T SRAM

But the conventional 6T SRAM have stability limitations at low supply voltages. Hence we go for 8T SRAM design. It has the advantage of low power at read '1' operation. As it does not consume power at read '1' cycle.

3. PROPOSED DESIGN

3.1 Need of Schmitt Trigger Based SRAM Designs

In order to reduce the read versus write design requirements in the conventional 6T bit cell, we apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the proposed ST SRAM bit cells, the feedback mechanism is used only in the pull-down path, as shown in figure. During input transition 0->1 the NF transistors makes the nmos logics at pull down of inverter to operate at high switching threshold thus achieves sharper characteristics During input transition 1->0 the feedback will not be present which makes smoother characteristics.

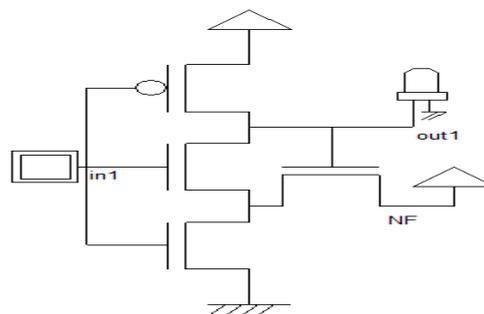


Figure 2: Schmitt trigger

Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bit cell. Two novel bit cell designs are proposed. The first ST-based SRAM bit cell has been presented in our earlier work. Another ST-based SRAM bit cell which further improves the bit cell stability has been reported in existing works. To maintain the clarity of the discussion, the ST bit cell in [30] is termed the "ST-1" bit cell while the other ST bit cell is termed the "ST-2" bit cell shown in the Figure below.

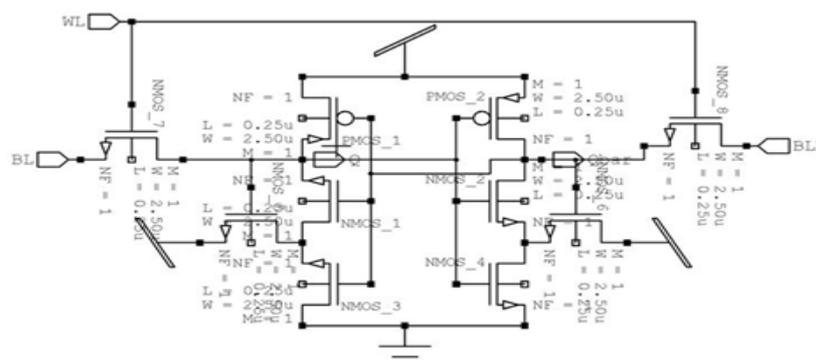


Figure 3: ST1 Bit Cell

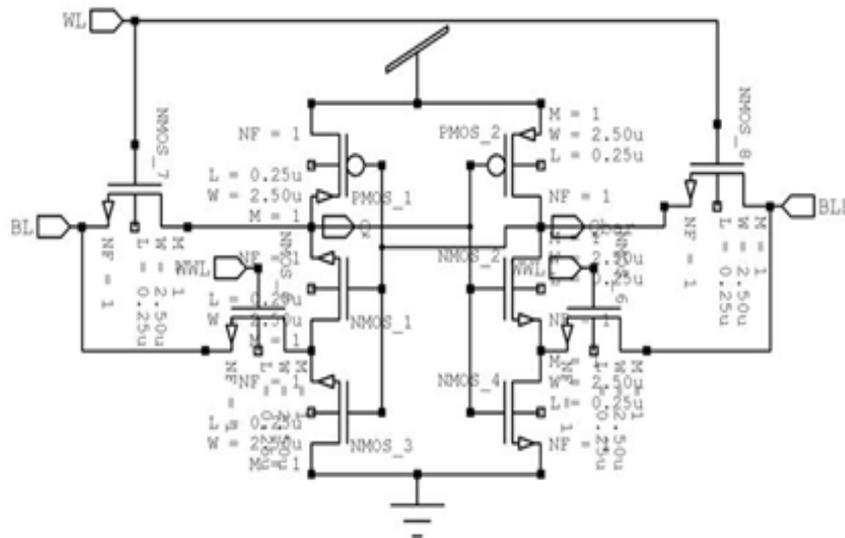


Figure 4: ST2 Bit Cell

Table 1: Operation of SRAM cell

	WL	WWL
Write	0	1
Read	1	0
Hold	0	0

The inverter change shown in above fig:2 improves the characteristics of the SRAM network. The above shows the ST-1 cell and ST-2 cell difference was the in ST-1 feedback was provided in only one cycle because the input of feedback transistor was depends upon the output of data once output data start changes the feedback transistors also lost. ST-2 improves characteristics by using separate Word Line WWL.

3.2 Negative bias temperature instability

NBTI is a key reliability issue in MOSFETs. It is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage; however, the very same mechanism affects also nMOS transistors when biased in the accumulation regime, i.e. with a negative bias applied to the gate too. NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and trans conductance. The degradation exhibits logarithmic dependence on time. This NBTI makes PMOS threshold voltage to increase. In order to reduce this NBTI problem of SRAM network here we introduce a recovery boosting technique. In recovery boosting technique SRAM operates in two modes of operation by switching CR line. One was normal mode which acts like normal SRAM network and another was recovery mode which makes PMOS to off and acts like a recovery transistor.

Here we apply recovery boosting technique to Schmitt Trigger SRAM network.

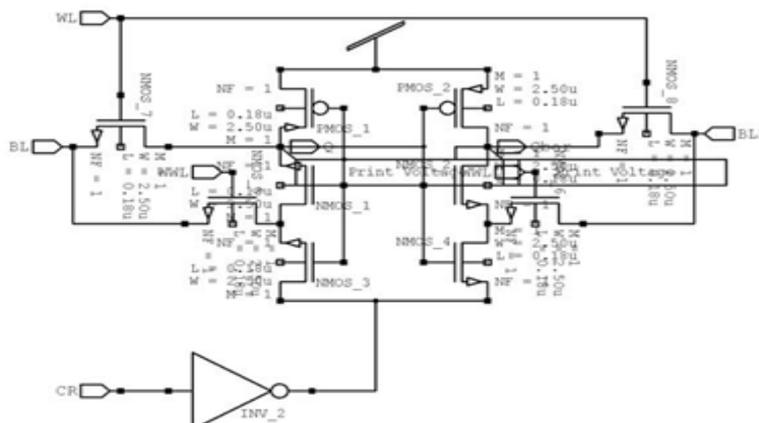


Figure 5: Schmitt Trigger SRAM with recovery Boosting.

4. SIMULATION AND RESULTS

These circuits are designed and simulated using Tanner EDA with TSMC018 technology

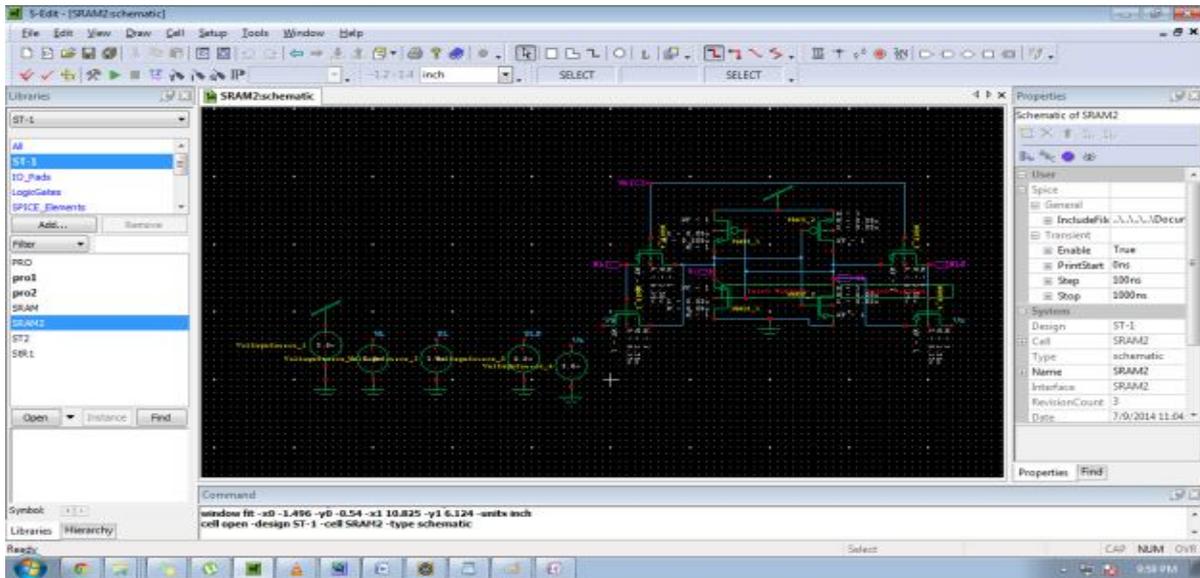


Figure 6: ST SRAM schematic design in S-Edit

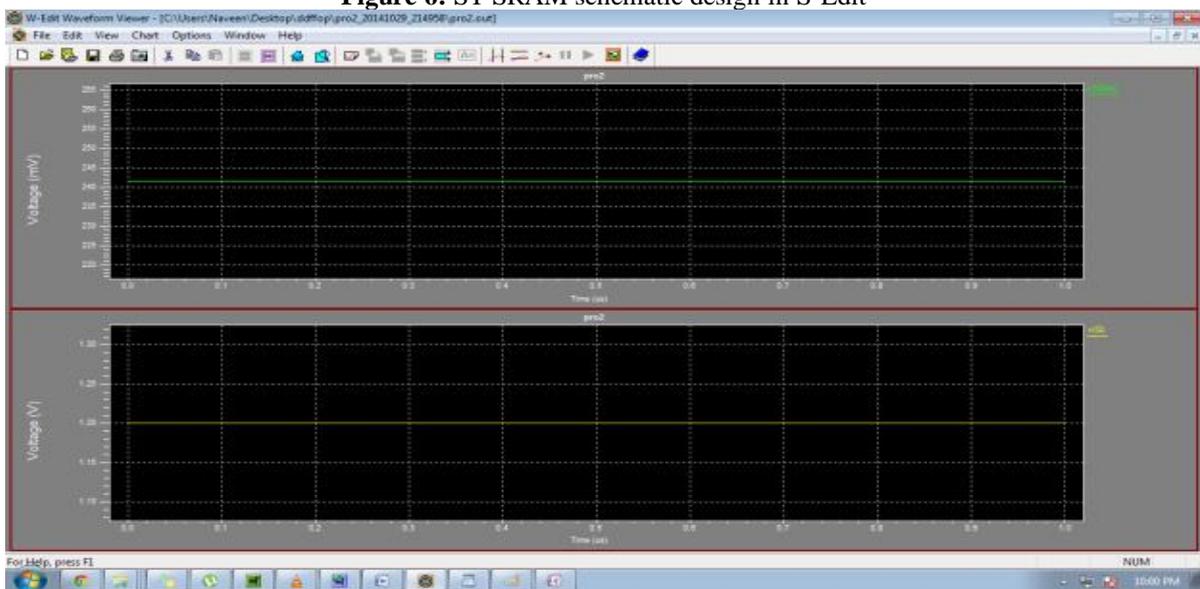


Figure 7: Simulation of ST-SRAM

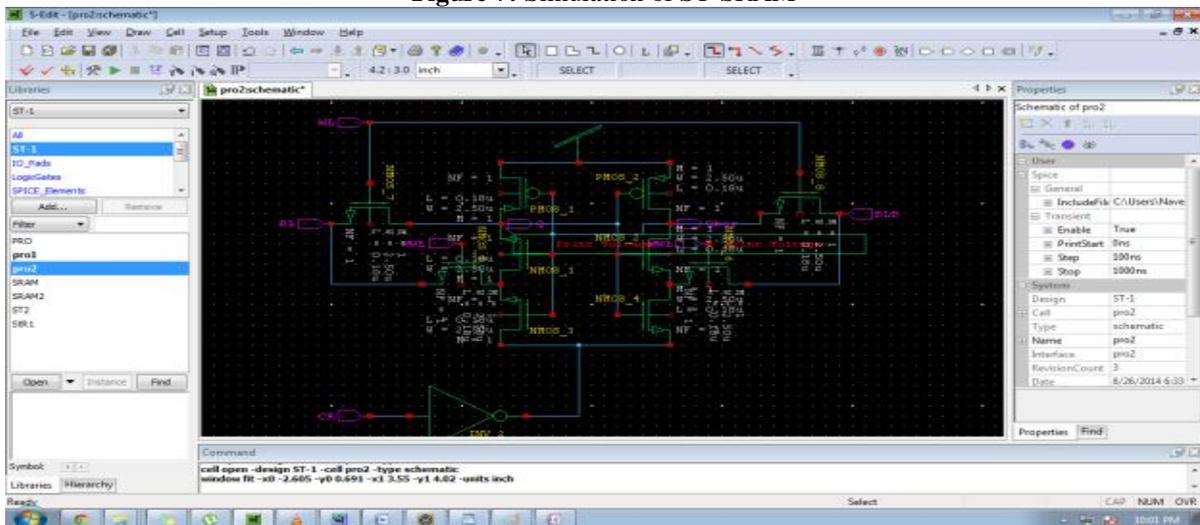


Figure 8: SRAM with recovery boosting

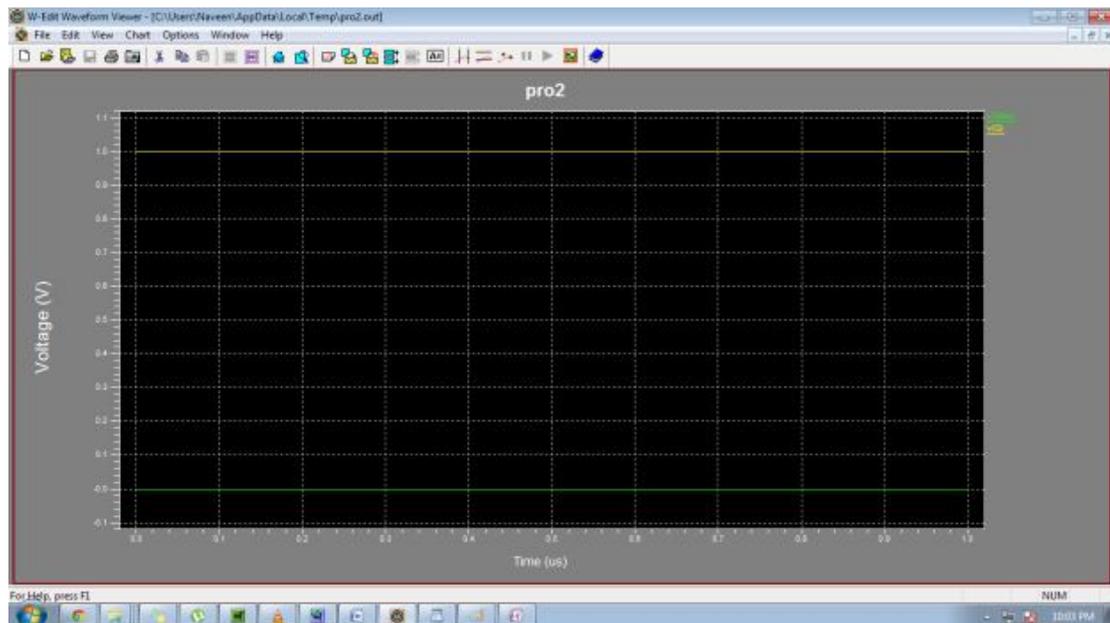


Figure 9: Simulation of SRAM with recovery boosting

5. CONCLUSION

Our proposed design shows that much less power than the existing ones 2.890uw at the standard Our Proposed layout combined with 6T & Virtual grounding with read error reduction Circuit concept 180nm technology. And it is having much reduced area than the conventional SRAM designs. Thus this design can be used for future SRAM core memories.

Reference

- [1] Kevin, Z., *Embedded Memories for Nano-Scale VLSIs*. 2009: Springer Publishing Company, Incorporated. 400.
- [2] Brown, A.R., Roy, G., and Asenov, A., Poly-Si-Gate- Related Variability in Decanometer MOSFETs With Conventional Architecture. *Electron Devices, IEEE Transactions on*, 2007. **54**(11): p. 3056-3063.
- [3] Bo, Z., et al. A Sub-200mV 6T SRAM in 0.13um CMOS. *in Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*. 2007.
- [4] Cheng, B., Roy, S., Roy, G., Brown, A., and Asenov, A. Impact of Random Dopant Fluctuation on Bulk CMOS 6-T SRAM Scaling. *in Solid-State Device Research Conference, 2006. ESSDERC 2006. Proceeding of the 36th European*. 2006.
- [5] Jawar Singh, D.K.P., Simon Hollis, and Saraju P. Mohanty, A single ended 6T SRAM cell design for ultra-low-voltage applications. *IEICE Electronics Express*, 2008. **5**(18): p. 750-755.
- [6] Mizuno, H. and T. Nagano, Driving source-line cell architecture for sub-1-V high-speed low-power applications. *Solid-State Circuits, IEEE Journal of*, 1996. **31**(4): p. 552-557.
- [7] Takeda, K., et al., A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications. *Solid-State Circuits, IEEE Journal of*, 2006. **41**(1): p. 113-121.
- [8] Chang, L., et al., An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High- Performance Caches. *Solid-State Circuits, IEEE Journal of*, 2008. **43**(4): p. 956-963.
- [9] Tae-Hyoung, K., et al. A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual Ground Replica Scheme. *in Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*. 2007.
- [10] Wang, X., Roy, S., and Asenov, A., Impact of Strain on the Performance of high-k/metal replacement gate MOSFETs, in *Proc. 10th Ultimate Integration on Silicon (ULIS 2009)*. 2009.