

Low Power Computing Logic Gates design using Reversible logic

p.Vanusha¹, k.Amurtha Vally²

¹P.G Student, VRS&YRN Engineering &Technology, vadaravuroad, Chirala

² Assistant Professor, VRS&YRN Engineering &Technology, vadaravuroad, Chirala.

ABSTRACT

Reversible logic has become one of the promising research directions in low power dissipating circuit design in the past few years and has found its applications in low power CMOS design, cryptography, digital signal processing, optical information processing and nanotechnology. This paper presents a quantum cost efficient reversible full adder gate and Reversible Decoder in nanotechnology. This gate can work singly as a reversible full adder & Decoder unit and requires only one clock cycle. The proposed gate is a universal gate in the sense that it can be used to synthesize any arbitrary Boolean functions. To implement reversible logic gates we are designing Full adder and Decoder circuit by using the T-Spice simulation and calculate the power consumption with TSMC018 Nanometer Technology.

Keywords :- Reversible logic, CMOS, Full adder, Decoder

1.INTRODUCTION

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. Irreversible hardware computation results in energy dissipation due to information loss. This paper presents a novel 4*4 reversible gate namely Peres Full Adder Gate (PFAG), that is, it has 4-input lines and 4-output lines. This gate can be used to realize any arbitrary Boolean function and therefore universal. The hardware complexity of this gate is less compared to the existing ones and requires only one clock cycle. The quantum realization cost of this gate is only 8 and ready for use in current nanotechnology. Reversible logic design differs significantly from traditional combinational logic design approaches. In reversible logic circuit the number of input lines must be equal the number of output lines, each output will be used only once and the resulting circuit must be acyclic. The output lines that are not used further are termed as garbage outputs. One of the most challenging tasks is to reduce these garbage's. Any reversible logic gate realizes only the functions that are reversible. But many of the Boolean functions are not reversible. Before realizing these functions, we need to transform those irreversible functions into reversible one. Any transformation algorithm that converts an irreversible function to a reversible one introduces input lines that are set to zero in the circuit's input side. These inputs are termed as constant inputs. Therefore, any efficient reversible logic design should minimize the garbage's as well as constant inputs. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one. Most of the energy needed to make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. It will impact instruction sets and high-level programming languages as well. Eventually, these will also have to be reversible to provide optimal efficiency

Irreversible & Reversible Logic Gates

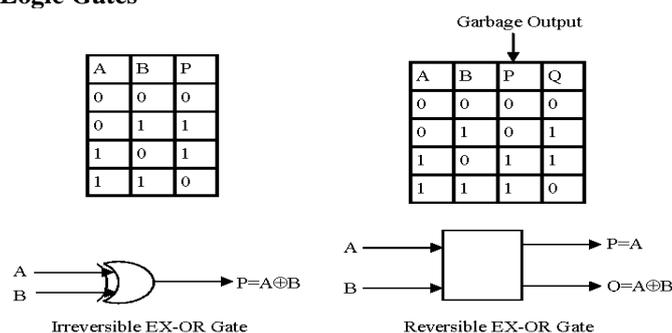


Fig 1: Irreversible & Reversible Logic Gates

MOTIVATION BEHIND REVERSIBLE LOGIC:

High-performance chips releasing large amounts of heat impose practical limitation on how far can we improve the performance of the system. Reversible circuits that conserve information, by un computing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. Reversible computing will also lead to improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits such as nanocircuits and therefore the speed of most computing applications. To increase the portability of devices again reversible computing is required. It will let circuit element sizes to reduce to atomic size limits and hence devices will become more portable. Although the hardware design costs incurred in near future may be high but the power cost and performance being more dominant than logic hardware cost in today’s computing era, the need of reversible computing cannot be ignored.

2.EXISTING DESIGN

2.1 REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one-to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

- i. The number of Reversible gates (N): The number of reversible gates used in circuit.
- ii. T: The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- iii. The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.

2.2 BASIC REVERSIBLE LOGIC GATES

2.2.1 Feynman Gate

Feynman gate is a 2*2 one through reversible gate as shown in figure 1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by $P=A$, $Q=A \oplus B$. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs

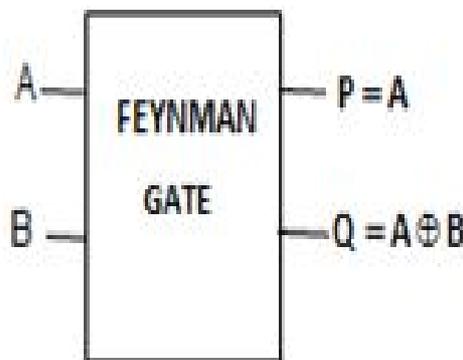


Fig2: Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Truth table of Feymans gate

2.2.2 Double Feynman Gate (F2G)

Fig.3 shows a 3*3 Double Feynman gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by $P = A$, $Q=A \oplus B$, $R=A \oplus C$.

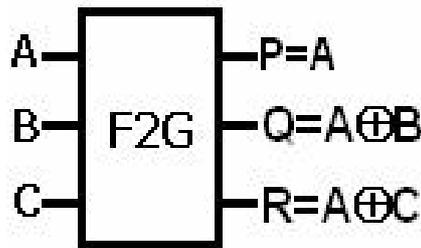


Fig3:Feynman Double Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Truth table of double Feynman gates

2.2.3 Fredkin Gate

Fig 4 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by $P=A$, $Q=A'B \text{ exor } AC$ and $R=A'C \text{ exor } AB$.

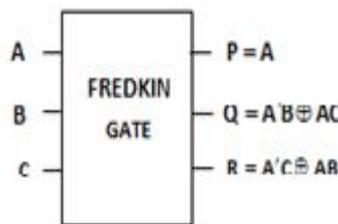


Fig 4: Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Truth table of fredkin gate

2.2.4 Peres Gate

Fig 5 shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by $P = A$, $Q = A \text{ exor } B$ and $R=AB \text{ exor } C$.

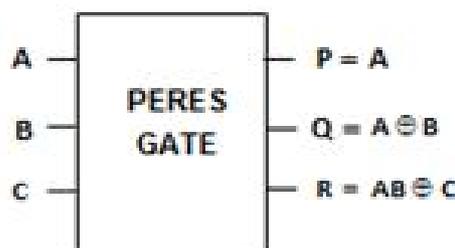


Fig 5: Peres Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Truth table of peres gate

3. PROPOSED DESIGN

3.1 Full adder using two Peres Gates

A full- adder using two Peres gates is as shown in fig .The quantum realization of this shows that its quantumcost is 8 two Peres gates are used. A single 4*4 reversible gate called PFIG gate with quantum cost of 8 is used to realize the multiplier

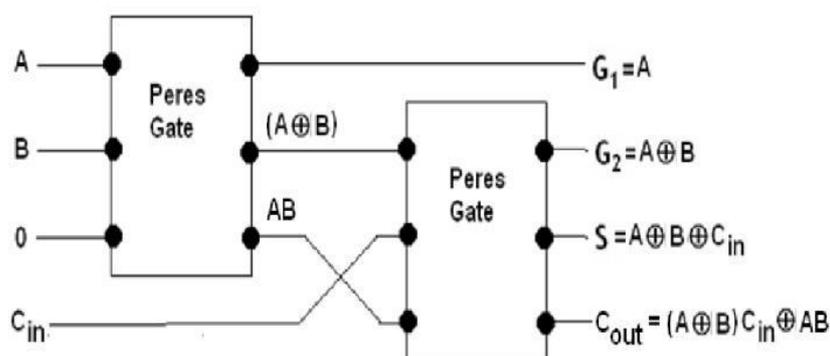


Fig 6:Full adder using two Peres gates

3.2 Decoder circuit using F2G gates and FRG Gates

A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. Decoders are the collection of logic gates fixed up in a specific way such that, for an input combination, all outputs terms are low except one. These terms are the minterms. Thus, when an input combination changes, two outputs will change. Let, there are n inputs, so number of outputs will be 2^n . There are several designs of reversible decoders in the literature. To the best of our knowledge, the designs from [1] is the only reversible design that preserve parity too.

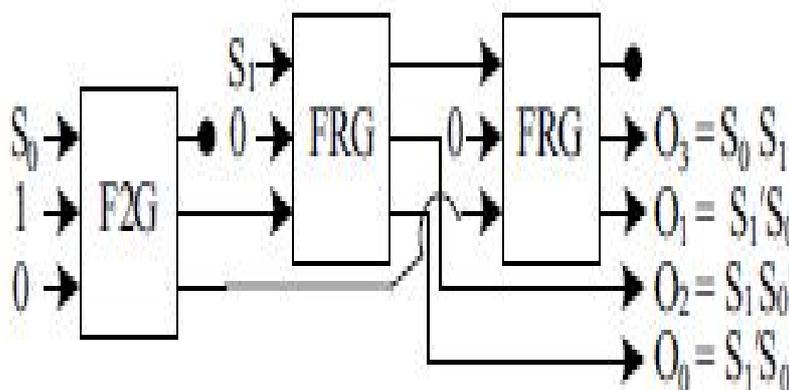


Fig 7:Reversible Logic Decoder

4. APPLICATIONS

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

1. Low power CMOS.
2. Quantum computer.
3. Nanotechnology
4. Optical computing
5. Design of low power arithmetic and data path for digital signal processing (DSP).
6. Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair

5. SIMULATION

These circuits are designed and simulated using Tanner EDA with TSMC018 Technology

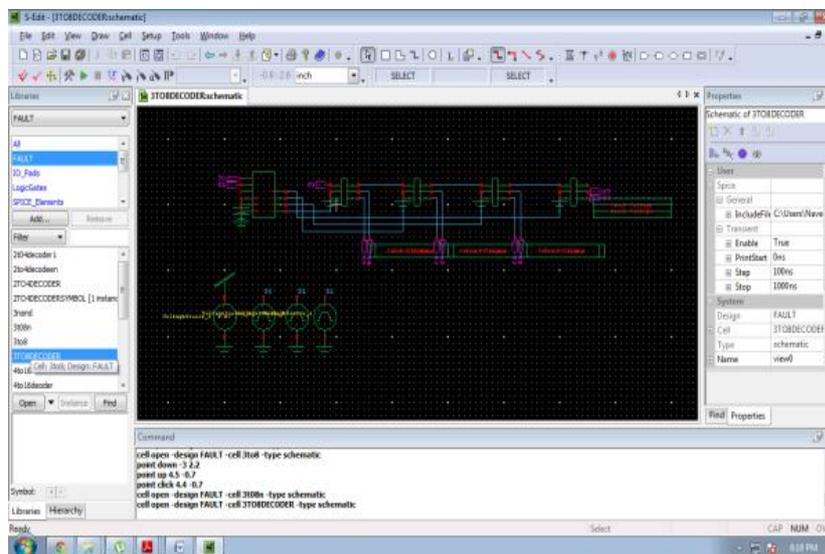


Fig 8: Design of 3 to 8 decoder

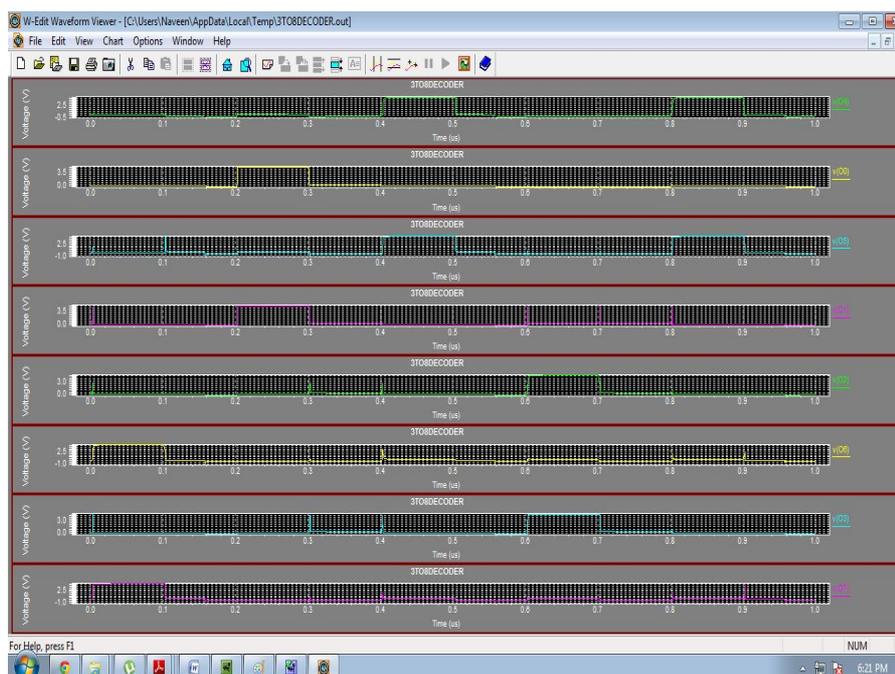


Fig 9: Simulation of 3 to 8 decoder

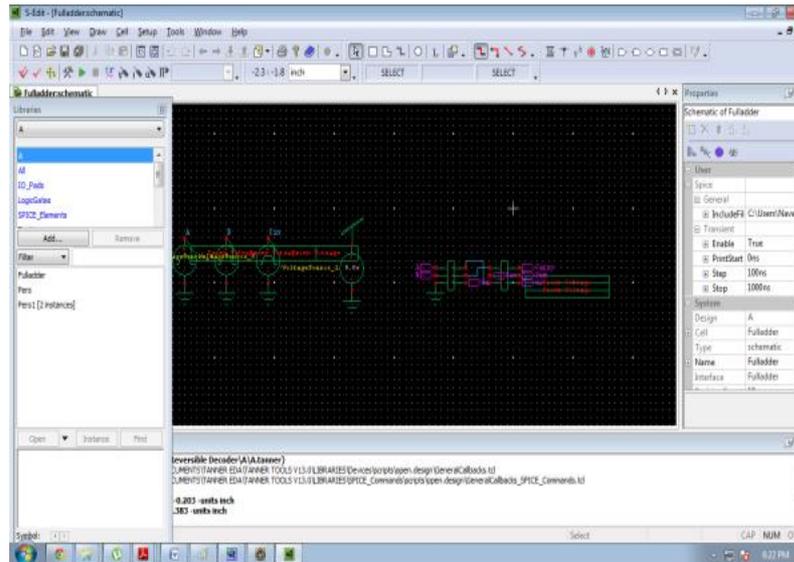


Fig10: Full adder design

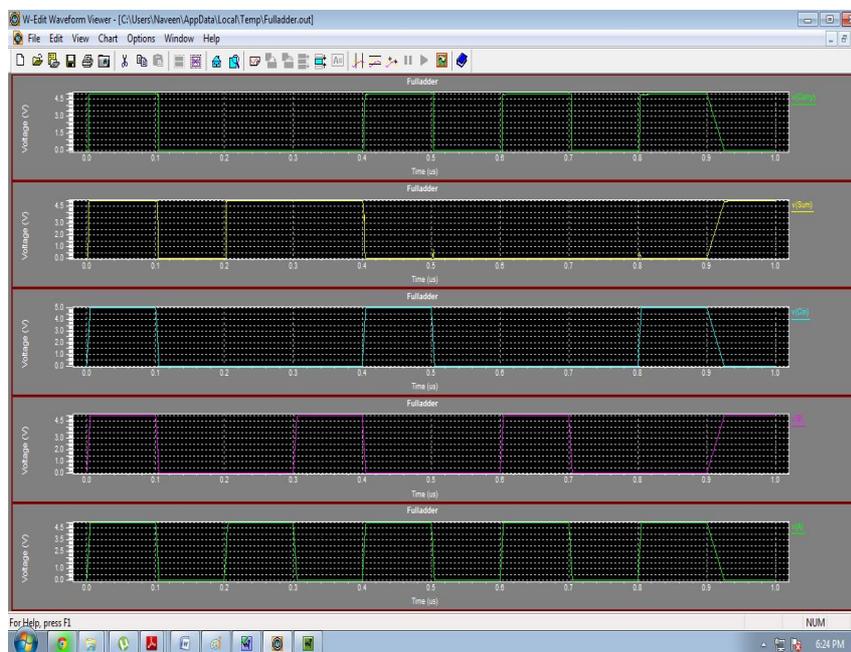


Fig 11: Simulation Full adder design

6. CONCLUSION

The reversible logic circuits play a very important role in design of low power digital circuits of a future computer. This has led many researchers to take reversible logic very seriously in building important circuits related to advanced computing, low power CMOS design. In this paper led to implement some of the reversible logic gates and their applications and their simulation results are shown by using Tanner EDA

7. FUTURE SCOPE

In this paper we work on the Reversible logic gates on combinational circuits in future we can extends these to implement this sequential circuits also

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