Abstract

The research work showed that the SOI MOSFET had excellent short-channel control from 0.4 to 2µm gate lengths and thin SOI devices could deliver high drive currents for logic applications and was better than the conventional structure. The basic of SOI MOSFET design process was studied with the help of ATLAS simulator and all the graphs showing the performance of undoped SOI n channel MOSFET were plotted using Tonyplot in SILVACO.

Keywords: TCAD, CMOS, MOSFET, SOI.

1. INTRODUCTION

For the high demand of faster and smaller electronic devices, the researchers and semiconductor manufacturers are putting a lot of effort to face the difficulties and challenges of improving the performance of the semiconductor devices from the conventional one.

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is largely known as popular device and is extensively used in digital circuits, microprocessors, memory circuit, and other logic applications. This device is used to amplify or switch electronic signals. The relative small size of MOSFET causes thousands of devices that can be fabricate into single integrated circuit design is other advantage to the electronic industry. The cost and size are main advantages of MOSFET devices.

Since the technology is well established, fabrication methods have become relatively inexpensive. Also, the device itself is physically smaller than other technologies, allowing for the placement of more devices on a silicon wafer during fabrication. MOSFET devices are mainly used in the creation of CMOS logic chips.

2. SILICON-ON-INSULATOR

SOI (Silicon-On-Insulator) [1] devices are a relatively new technology. Although the technology has been around since the 1960’s, SOI devices are only recently becoming commercially viable, due to the expense associated in producing the devices. SOI devices are an advancement of standard MOSFET technology.
2.1 DIFFERENCE BETWEEN SOI AND MOSFET

The main difference between SOI and MOSFET technology is the inclusion of an insulating layer. In Silicon on Insulator (SOI) fabrication technology Transistors are built on a silicon layer resting on an Insulating Layer of Silicon dioxide (SiO$_2$). The insulating layer is created by flowing oxygen onto a plain silicon wafer and then heating the wafer to oxidize the silicon, thereby creating a uniform buried layer of silicon dioxide. Transistors are encapsulated in SiO$_2$ on all sides. This structure is shown in figure 2.

Most often this material is silicon oxide; however other insulating materials are being tested, such as diamond, sapphire, and ruby. For this, a buried oxide layer (BOX) of silicon dioxide was used for the creation and simulation of the SOI device. The insulating layer increases device performance by reducing junction capacitance as the junction is isolated from bulk silicon. The decrease in junction capacitance also reduces overall power consumption.

![Figure 2 Physical structure of basic SOI device](image)

2.2 SOI TECHNOLOGIES

SOI technologies can be in general divided into two groups. In the first, a thin insulating layer is used to separate the active semiconductor layer from the semiconductor substrate. These include Separation by Implantation Of Oxygen (SIMOX), Zone Melting Recrystallization (ZMR), Full Isolation by Porous Oxidized Silicon (FIPOS), and Wafer Bonding (WB). In the second group, the semiconductor film is deposited directly onto an insulating substrate. This is the case for Silicon On Sapphire (SOS) and Silicon On Zirconia (SOZ).

2.3 SOI ADVANTAGES

1. A 20% to 50% increase in switching speed compared to similar circuits built on conventional "bulk" silicon wafers.
2. The ability to operate at lower voltages (less battery power drain and chip heating).
3. Events from cosmic ray particle showers (reducing the need for error correction operations in high-speed data flow servers and memory arrays).
4. Increased circuit packing due to simplification of the lateral and vertical isolation structures, increasing chip yield and die count per wafer.

3. THEORY ON TCAD TOOLS

Technology Computer Aided Design (TCAD) simulation tools is a virtual software fabrication and operation simulation of semiconductor devices. This TCAD simulation tools is used to plan, design and test the device structure such as MOSFET before the actual fabrication process. This test is important in order to assist researcher in designing device structures and investigating the overall device performances based on device characteristics that have been extracted from the device simulation (ATLAS) results. Besides that, TCAD simulation tools also can reduce time constrained and save cost compare to actual fabrication process.

DeckBuild is the front-end GUI (Graphical User Interface) for Silvaco’s Virtual Wafer Fabrication programs. This program is the framework which ties together the wide range of process and device simulation tools available, and allows them to work together seamlessly and efficiently. DeckBuild uses pull-down menus to generate syntax for the various programs, and provides basic simulation controls such as stop, pause, and restart.

ATLAS is a device simulation tool and the framework of which combine several one, two, and three-dimensional simulation tools into one comprehensive device simulation package. SOI nMOSFET can be created in ATLAS through layout based simulation syntax[5]; however the main focus of the program is simulation of the device once fabrication is complete.
4. DEVICE STRUCTURE

The thickness of the silicon layer in a partially-depleted device is 2µm and the thickness of the BOX should be thick enough to block the current. The n-type doping in the drain and source regions is taken 1x10^{29}cm^{-3}. Then the p-type doping in the silicon, which mostly affected the doping level in the area under the gate is taken 6x10^{17}cm^{-3}. The gate length [6] is taken as 2µm wide, keeping it centered in the device. The overall length of the device is 3µm. The results were plotted and viewed using Tony Plot.

![Tony Plot of the SOI-NMOS device](image)

5. RESULTS AND DISCUSSIONS

Figure 4 shows the graph obtained which is the curve between drain current and gate voltage. It is seen that at the beginning, as the gate voltage is increasing, the drain current is not increasing. The variation of gate voltage from 0.1V to 0.9V shows that there is no change in the drain current. But as soon as the gate voltage reaches to 1V, the drain current starts increasing at a lower rate. When the gate voltage increases beyond 1V then the drain current also increases along with it. Hence, it is seen that from 0.1V to 0.9V, there is no change in drain current i.e. the curve is non linear but after 0.9V gate voltage, we get a linear curve or response. Thus, there is a sudden rise in the value of drain current after a particular value of gate voltage is reached.

![I_D-V_G curve of SOI-NMOS](image)

Firstly, the thickness of the silicon layer was varied from 0.05µm to 2µm, changing it from a thin fully depleted device to a partially-depleted device. As the silicon layer thickness increased, the thickness of the BOX also increased to block the current. After the effect of the silicon thickness was seen, it was set back to 1µm and the gate length was varied. This affected the length of the channel under the gate. Gate length was varied from about 0.4µm wide to 2µm wide, keeping it centered in the device. The overall length of the device, 3µm, was not changed. As it is seen in the figure 5 that as the thickness of the silicon layer is increased, the threshold voltage is also increased, and changing the silicon thickness really had no effect on the slope, which can be seen from the graph.

![Effect of silicon thickness on threshold voltage](image)
As shown in the figure 6 that when the gate length and channel area are increased, there is a slight increase in the threshold voltage, and the slope decreases. However, when the channel area gets below 0.6µm, the device is subject to short channel effects, and does not work properly. At this small size, the device becomes subject to quantum physics, and no longer acts the same way larger sized devices do, as seen by the odd results obtained at a gate length of 0.4µm.

Figure 6 Changing the gate and channel length

From the results obtained in the simulation design of an optimized device is possible in which the threshold voltage was closest to 0, and the slope was as linear as possible. By noting the effects the different parameters had on these two characteristics of the \( I_D - V_G \) curve, values could be chosen to give the best device. A graphical comparison of the original and optimized devices is shown in the figure 7 below. The optimized device has a much lower threshold voltage with a value quite close to 0 V, with a slope which is almost two times greater than that of the original device.

Figure 7 Threshold voltage comparisons for optimized and original SOI devices

6. CONCLUSION

It is concluded that, the proposed structure is better than the conventional structure. Each time parameters of the device were altered, the simulated device’s performed according to the equations and characteristics that would be expected from the device. This performance on parameters can be calculated and simulated. The characteristic are verified.

REFERENCES


AUTHOR

Anil Kumar is Assistant Professor at SHIATS-DU Allahabad. He obtained B.E from MMMEC Gorakhpur in ECE, M.Tech. from IIT BHU Formerly IT B.H.U. Varanasi in Microelectronics Enng. and presently pursuing Ph.D. from SHIATS-DU Allahabad. He guided various projects & research at undergraduate & postgraduate level. He published many research papers in different journals. He has more than 10 years teaching experience and actively involved in research and publications. His area of interest includes Antenna, microwave, artificial neural network and VLSI.
Ankita Kar is student of M.Tech. ECE (CSE) in the Department of Electronics & Communication Engineering in SHIATS-DU, Allahabad. She received her B.Tech degree from BBS CET Allahabad, U.P. Technical University, Lucknow.

A.K. Jaiswal is Prof. and Head of ECE-Dept at SHIATS-Allahabad. He obtained M.Sc. in Tech. Electronics & Radio Engg. from Allahabad University in 1967. He guided various projects & research at undergraduate & postgraduate level. He has more than 40 years Industrial, research and Teaching experience and actively involved in research and publications. His area of interest includes Optical Networks and satellite communication.

Nivedita Kar is student of M.Tech. ECE (CSE) in the Department of Electronics & Communication Engineering in SHIATS-DU, Allahabad. She received her B.Tech degree from BBS CET Allahabad, U.P. Technical University, Lucknow.