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FPGA INTERFACE FOR AN ANALOG INPUT MODULE

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ABSTRACT

The project is intended to read the analog data from the field sensors to the ADC Evaluation Board through FPGA interfacing and store the data into memory. VHDL code is developed to program the FPGA. The analog input required by the ADC's is given through a single multiplexer. ADC converts the analog data into digital input and sends to the MCU. MCU processes the received digital input and the processed data is sent to the FPGA through serial peripheral interface (SPI). The FPGA is programmed using VHDL Language for interfacing the MCU unit for configuring the ADCs and read the field data converted to digital by the ADCs. Serial peripheral interface is an interface which interfaces master and slave. In this Project microcontroller acts as a master and FPGA acts as a slave, because always master initiates data transfer. SPI is a serial interface that allows eight bits of data to be synchronously transmit and simultaneously receive, that is, full duplex. The SPI port consists of four pins: MISO, MOSI, SCL, and CS.In This project we using SPARTAN SP601 FPGA (Spartan®-6 XC6SLX16-2CSG324). Input voltage levels of the Analog Input module is ±7.8125 mV to ±1.2V and the basic advantages are economical, high precision. In this paper we are going to discuss about interfacing microcontroller of ADC Evaluation board and FPGA with SPI.

Keywords: ADC Evaluation Board, SPARTAN SP601 FPGA, serial peripheral interface (SPI)

1. INTRODUCTION

In this project we are designing the universal analog input module of the programmable logic Controller (PLC); here the input may be voltage or current. The input voltage range of the analog input module is ±7.8125 mV to ±1.2V .Analog input module is the interface between field sensors and PLC. Field sensors are RTDS (Resistance temperature detector) and Thermocouple devices.

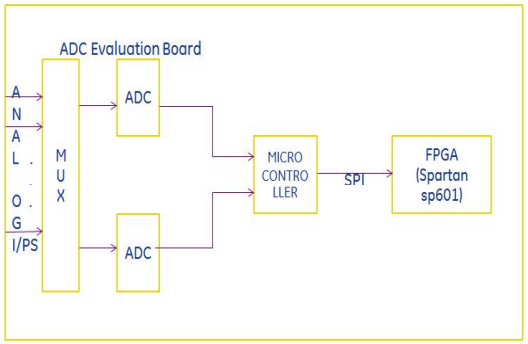


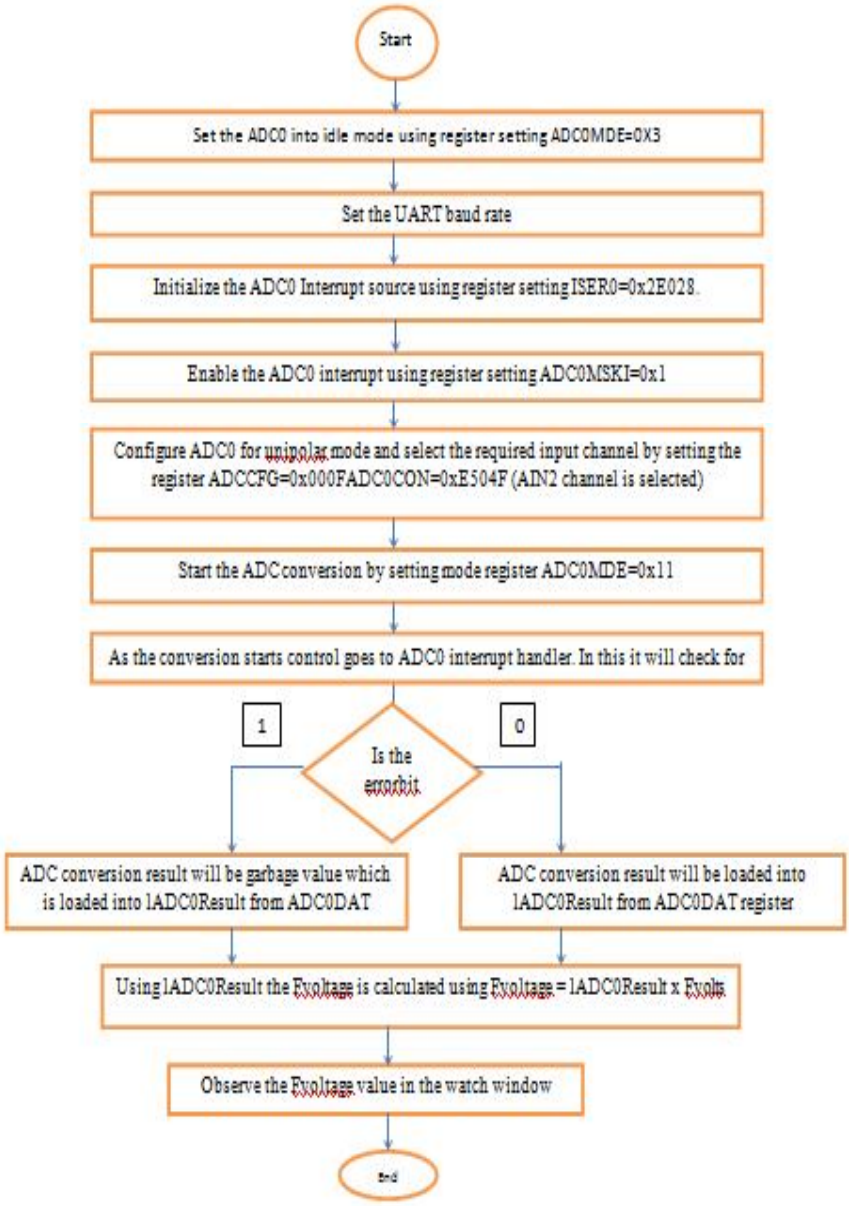
Fig1: Interfacing of two modules

2. METHODOLOGY

Read the analog input data through 11 channels by using memory mapped registers of ADC and the corresponding data are stored in the microcontroller. Processed digital data has to go to the FPGA, So interface the microcontroller and FPGA by using serial peripheral interface. For the above interface develop the VHDL code for FPGA.

3. ANALOG INPUT MODULE

The ADC Evaluation board has one IC from ADI which has following internal components: flexible Input multiplexer, two 24 bit ADCs (analog to digital converters), 32 bit microcontroller unit (MCU), on chip peripherals.fig 1shows Flow chart for reading ADC channel data



SPI Master (microcontroller)

The microcontroller output which is digital, given by 1ADC0Result variable is sent to FPGA through SPI interface. The interfacing is done by configuring the microcontroller SPI pins. The SPI MISO pin register (GP1CON) is set to 0x200. The SPI MOSI pin register (GP1CON) is set to 0x2000. Set the chip select pin register (GP1CON) to 0x800 and SPI CLK pin register to 0x8000.SPI clock frequency is set using register SPI0DIV=0x0080 and the SPI control register (SPI0CON) is set to 0x0ACB.The digital value is masked by splitting the result into 1 byte each because, the SPI transmit register supports single byte data transfer at a time. These bytes are stored in user defined variables A, B, C, D.SPI master result is shown in the fig 3.

SPI SLAVE (FPGA)

The evaluation board digitizes the required analog input and sends to FPGA through serial Peripheral interface (SPI).the FPGA programming is carried out in the following way: In SPI interface FPGA acts as a slave. Chip select is an active low signal, if chip select(CS) is '1' then no of bits are received to FPGA(i.e. no transmission occurs).if CS is '0'then data received from microcontroller through MOSI line, and store the 32 bit data into data_rxd register. Count signal is used for checking whether the 32 bits received or not. Using UART, data is displayed on the terminal window.

Result

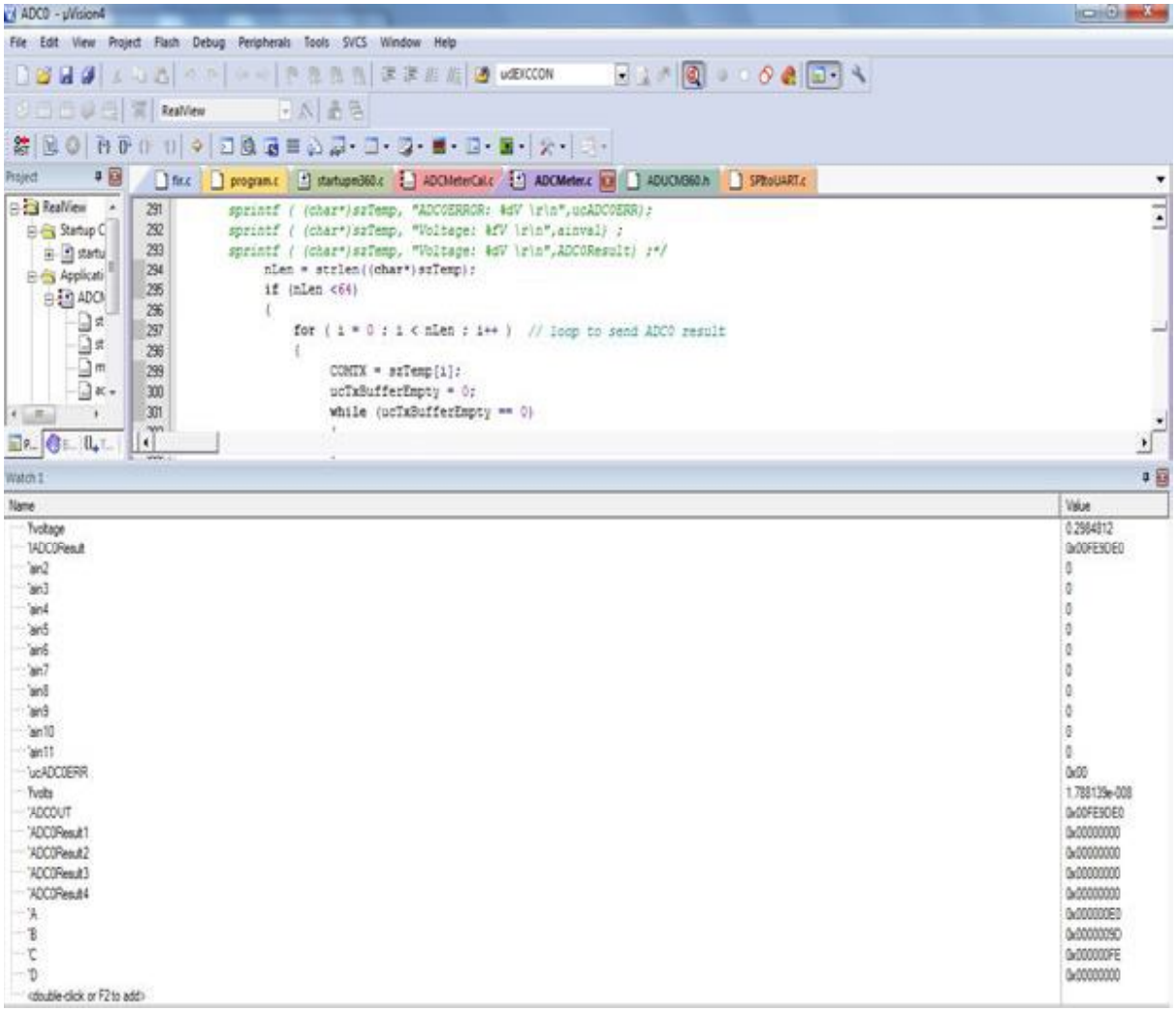


Fig 3: Result of SPI master(**microcontroller)**

Flow Chart of SPI SLAVE (FPGA)

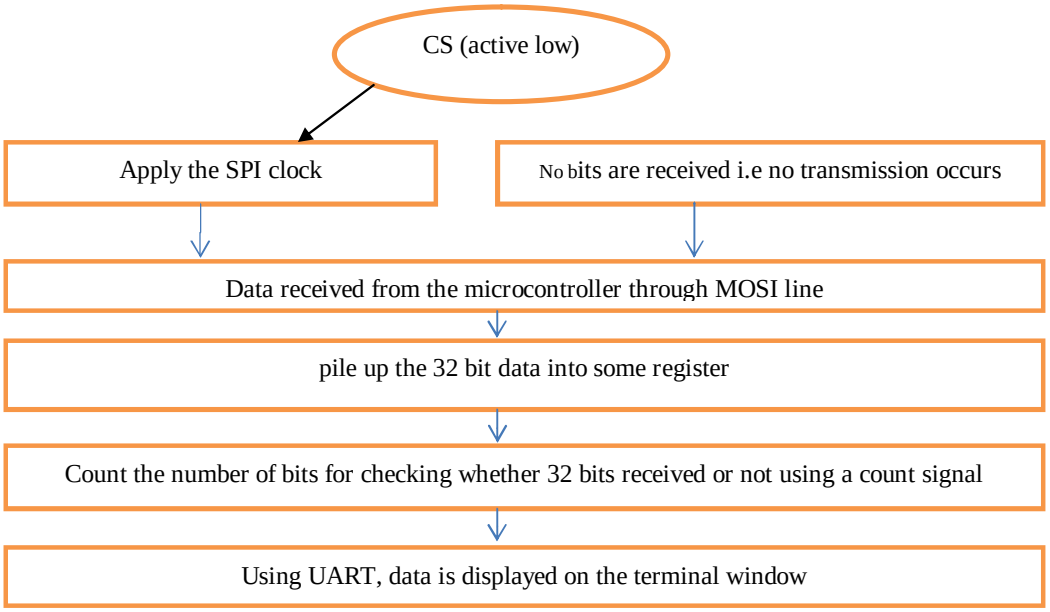


Fig 4: Flow Chart of SPI SLAVE (FPGA)

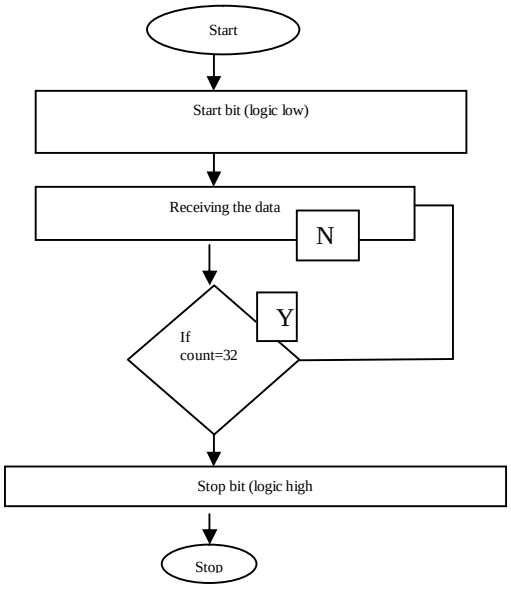
UART Transmitter

1. Generate the UART clock with the baud rate of 115200 from 27 MHz clock of FPGA.
2. When the Tx_start signal is high then transmission starts
3. Data load procedure:
   Tx_Data is sent into a data signal
4. for data transmission:

If start=0 it indicates that start of the data transmission. Then bit by bit transmission of the data starts. If the stop bit=1 then indicates completion of data.

UART Receiver

32 bit data is received by using UART receiver and displayed on the terminal window. Fig5: Flow chart of UART Receiver



Project Setup

Fig 5: UART Receiver

General purpose IO pins (F15, B4, F13, P12) are used to configure the MISO, CLK, MOSI, CS pins respectively. Flow chart indicates the process of receiving data by FPGA and this received data is displayed on the terminal window by using UART.

Result of SPI slave

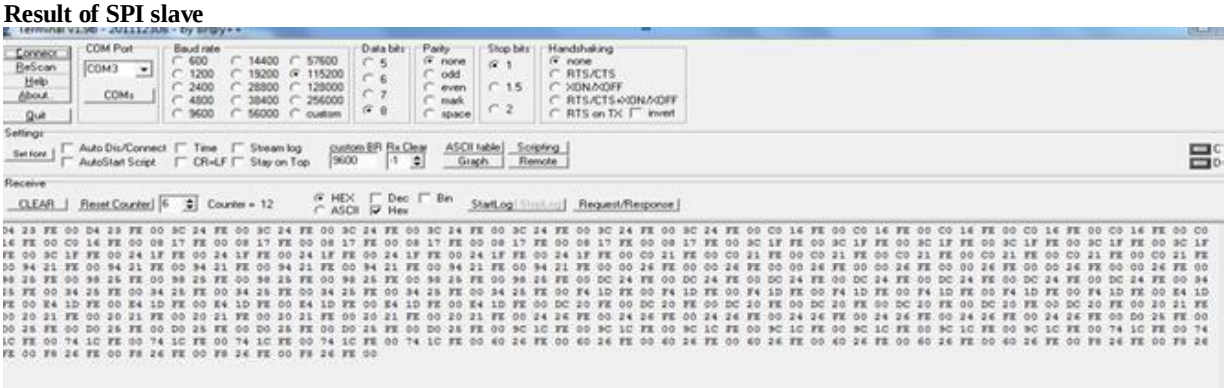


Fig7: Result of SPI slave

ADC Registers

1. ADC Control Register(ADCxCON)

Bit Descriptions for ADCxCON

Table1: Bit Descriptions for ADCxCON

Bits	Name	Description	Bits	Name	Description
31:20	Reserved		14	BUFBYPN	Negative buffer bypass. 1: Negative buffer bypassed

					0: Negative buffer not bypassed
19	ADCEN	Enable Bit. 1: Enable the ADC 0: Power down the ADC, ADCxRDY bit is cleared	13:12	ADCREF	Reference selection. 00:INTREF-AGND , 01:EXTREF (The external buffer mode is set in the ADCxCFG register) , 10:EXT_REF2IN (Valid only for ADC1). EXT_REF2IN+ Buffer controlled via ADCxCFG), 11:AVDD-AGND
18	ADCCODE	ADC Output Coding. 1: Unipolar 0: 2's complement (Bipolar) This bit also affects the coding of the Accumulator (ADCxACC) and ADCxTH.	[11:10]	ADCDIAG	Diagnostic Current bits. 00 : Current Source Off , 01 : Enable ISRC Current (50µA) on selected positive input (e.g. Ain0), 10 : Enable ISRC Current (50µA) on selected negative input (e.g. Ain1) 11 : Enable ISRC Currents (50µA) on selected input (e.g. Ain0 & Ain1)
17	BUFPOWN	Negative buffer power. 1: Negative buffer power down 0: Negative buffer enabled	[9:5]	ADCCP	Positive input channel selection: 00000: Ain0, 00001: Ain1\ ... ... , 01011: Ain11 , 01111: AGND , 11100: All channels off (default) for Auxiliary ADC (ADC1)only: 01100: DAC output 01101: AVDD/4: 01110, IOVDD/4: 01111: 10000: Temperature sensor 11111: All channels off (default)
16	BUFPOWP	Positive buffer power. 1: Positive buffer power down 0: Positive buffer enabled	[4:0]	ADCCN	Negative input channel selection: 00000: Ain0 , 00001: Ain1 ... ... ,01011: Ain11 , 01111: AGND 01100: All channels off (default) for Auxiliary ADC (ADC1) only: 10001: Temperature sensor For all other internal channel measurements select AGND
15	BUFBYPP	Positive buffer bypass. 1 : Positive buffer bypassed 0: Positive buffer not bypassed			

2. ADC Mode control registers (ADCxMDE)
Bit Descriptions for ADCxMDE:

Table2: Bit Descriptions for ADCxMDE

Bits	Name	Description
[15:8]	Reserved	
[7:4]	ADCxPGA	PGA Gain Select bit. 0000 PGA Gain = 1, 0001 PGA Gain = 2, 0010 PGA Gain = 4 , 0011 PGA Gain = 8, 0100 PGA Gain = 16, 0101 PGA Gain = 32, 0110 PGA Gain = 64, 0111 PGA Gain = 128, 1000 to 1111 Reserved
3	ADCMOD2	Modulator Gain of 2. This bit amplifies the output of the PGA by 2 for better resolution. 0: Modulator gain of 2 is disabled , 1: Modulator gain of 2 is enabled
[2:0]	ADCMD	ADC Mode bits. 000: ADC Power-Down Mode: The ADC circuitry is powered off. This powers down the ADC and PGA. Note: Allow 7us software delay before powering down the core 001: Continuous Convert Mode: The enabled ADC(s) continuously produce conversions at FADC. RDY must be cleared to enable new data be written into ADCxDAT. 010: Single Convert Mode: This performs a single-shot conversion on the enabled ADC(s). The ADC enters IDLE mode after RDY is set. 011: Idle Mode: The ADC is powered up but held in reset. Entered after calibration. 100: Self-Offset Calibration: An offset calibration is performed with an internally generated 0V. The input of ADC is a short to the negative pin of the selected channel. The result is written to the ADCxOF register of each enabled ADC. 101: Self-Gain Calibration: A gain calibration is performed with an internal/external VREF. For gain>=4, VREF is applied to an oon-chip resistor divider. If Gain>1, the Gain=1 coefficients must be in the Gain register. Self-Gain-Calibrations take 2X longer if the PGA Gain is >= 2. 110: System-Zero-Scale Calibration. ADC offset calibration on selected channel; the channel should be short externally. 111: System-Full-Scale Calibration. User to add correct FS voltage to input pins.

Advantages

1. Economical
2. Precision is high
3. Space of the BOM (bill of material) is reduced because components are reduced.

Application areas

1. Industrial Automation and precision sensing system.
2. Industrial applications that use analog input card as the input module.
3. 4-20 ma loop powered instrument - Pressure/flow/temperature
4. Remote Automation.
5. Controllers and I/O.
6. Industrial Computing.
7. To read the data from the temperature sensor (RTD or thermocouple devices)

4. Conclusion

Analog data is read through analog channels, micro controller of ADC evaluation board is interface with FPGA using Serial Peripheral Interface and the data is sent from microcontroller to FPGA using VHDL.

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AUTHOR

Ujwala Bollampalli received her Bachelor of Technology in Electronics and Communication Engineering from JNTU Hyderabad in 2009 and Master of Engineering in Digital Systems Engineering from Osmania University in 2012 and she presently working as a Assistant Professor in SR INTERNATIONAL INSTITUTE OF TECHNOLOGY, Hyderabad, INDIA and she had a interest in the field of Design for Tolerance and VLSI Technology for her research.