International Journal of Application or Innovation in Engineering & Management (IJAIEM)
Web Site: www.ijaiem.org Email: editor@ijaiem.org, editorijaiem@gmail.com
ISSN 2319 - 4847
Special Issue for National Conference On Recent Advances in Technology and Management for Integrated Growth 2013 (RATMIG 2013)

Voltage Sag Mitigation Using Three level Cascaded H-Bridge Multilevel Inverter based DSTATCOM in Low Voltage Distribution System

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ABSTRACT

In modern information society requirements and expectations associated with power quality have become increasingly important. Among the different disturbances affecting the power quality, the voltage sag are considered as a most important power quality problem faced by utilities & industrial consumer & equipment like PLC (Programmable Logic Controller), ASD (Adjustable Speed Drives) which need to be fully investigated. Custom power device are effective means for mitigating the voltage related issues prominently voltage sag, unbalanced load voltage, voltage regulation, sag/ swell etc. by compensating the reactive power with the injection of shunt current. In this paper by using three level H-bridge topology cascaded multilevel inverter based DSTATCOM the voltage sag is compensated effectively.

Keywords: *Cascaded Multilevel Inverter, DSTATCOM, Power Quality*

1. INTRODUCTION

POWER quality is becoming recently more important issue. Any power problem manifested in voltage, current, or frequency deviation that results in failure or disoperation of customer equipment is a Power Quality (PQ) problem. Nowadays load equipment is more sensitive to power quality variations than equipment used before, because in order to improve power system efficiency there is continuous growth in the application of devices with micro-processor and power electronics control[1].

Out of different power quality problems, such as transients, voltage fluctuations, harmonics, inter-harmonics, voltage unbalance, waveform distortion, dc offset, noise, notches etc. Voltage sag is one of the problems related to power quality [2].Various methods have been applied to reduce or mitigate the PQ problems. The conventional methods are by using capacitor banks, introduction of new parallel feeders and by installing Uninterruptible Power Supplies (UPS). However, the PQ problems are not solved completely due to uncontrollable reactive power compensation and high costs of new feeders and UPS. Another compensating system has been proposed by employing a combination of SVC and active power filter, which can compensate three phase loads in a minimum of two cycles. Nowadays, sensitive equipment's are being used in industries and the voltage sag in the power system is not acceptable. There are several methods that are being used to reduce the voltage sag. In some methods, compensators based on the voltage and current source are used thus, a controller which continuously monitors the load voltages and currents to determine the right amount of compensation required by the system and the less response time should be a viable alternative. Distribution Static Compensator (DSTATCOM) has the capacity to overcome the above mentioned drawbacks by providing precise control and fast response during transient and steady state, with reduced foot print and weight. The DSTATCOM (Distribution Static Compensator) has emerged as a promising device to provide not only for voltage sag mitigation but a host of other power quality solutions such as voltage stabilization, flicker suppression, voltage regulation, power factor correction and harmonic control [3].

DSTATCOM is a shunt type compensating device which is connected with distribution system. Suitable adjustment of the phase and magnitude of the DSTATCOM output voltages allows effective control of active and reactive power exchanges between the D-STATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power. The VSC connected in shunt with the ac system provides a multifunctional topology [4][5]. In this paper for voltage sag mitigation three-level H-Bridge topology is used which is found to be effective. Further three level H-bridge cascaded inverter with the effective control scheme [6][7] is used. It is found that

the voltage sag can be effectively mitigated using the proposed multilevel inverter based DSTATCOM with suitable control scheme.

2. PROPOSED DSTATCOM TOPOLOGY

Inverters are conventionally controlled as a PWM voltage source in medium and high-power applications because of switching losses. Since the converter is operated as a PWM voltage source, the switching frequency of the devices can be properly controlled. DSTATCOM is a FACTS device generating/absorbing the reactive power between ±QVAr. DSTATCOM consists of inverter, dc-link capacitor, coupling transformer/inductance and control algorithm. Inverter is the basic building of all converter based FACTS devices. Inverter used in power circuit of DSTATCOM must be operated at high switching frequency to response fast any changing in distribution systems. Besides, total harmonic distortion of inverter output voltage can be decreased depending on high switching frequency. Therefore, PWM inverters are more suitable for DSTATCOM application [8]. Recently, multilevel inverters have been used in DSTATCOM applications because of advantageous like direct connection to distribution system and improving the harmonic content of output voltage compared with conventional two-level PWM inverter operating in same switching frequency. Cascaded multilevel inverters among multilevel inverter topologies are the most popular topology because of using the least number of components and flexibility of circuit layout. In cascaded inverter, the number of output voltage levels can be easily increased by adding the H-bridges. The number of lowest voltage-level in the cascaded inverters is three. In addition, dc voltage unbalance doesn't occurred in three-level. In this paper three-level H-bridge inverter level cascaded

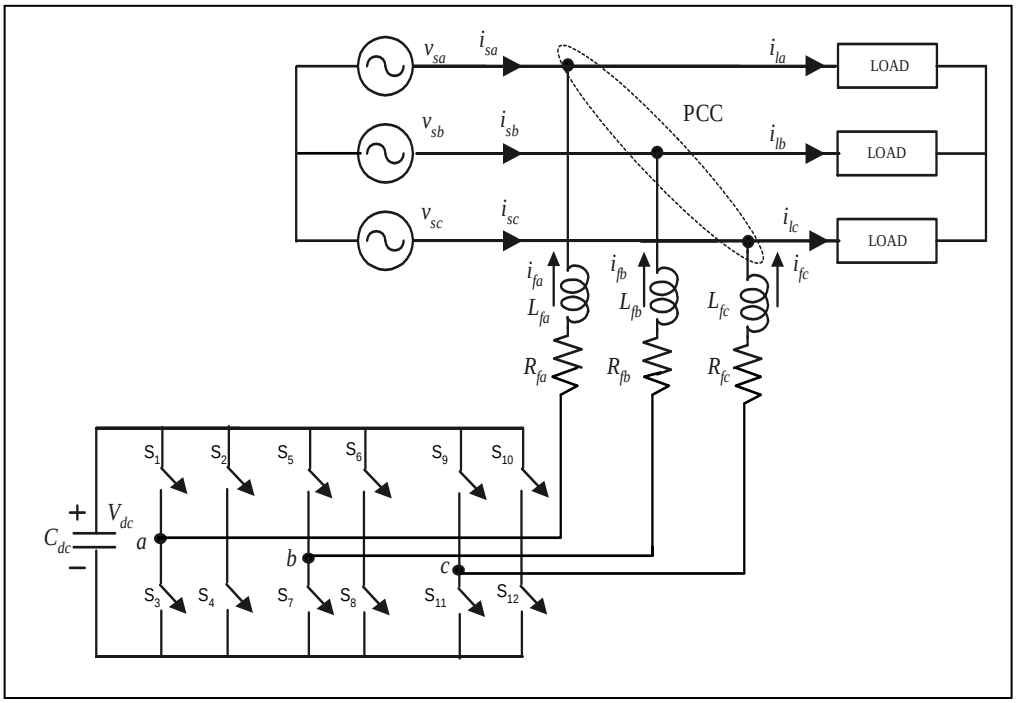


Figure 1. Three-phase, 3-level H-bridge inverter based DSTATCOM

H-Bridge inverter is preferred for power circuit of DSTATCOM. Flexible structure of this inverter easily allows increasing the number of voltage-level by adding the H-bridges in series to per phase. Power circuit of three-level H-bridge inverter based DSTATCOM is illustrated in Figure 1. DSTATCOM consists of three H-bridge inverters, dc-link capacitors (C)supplying the dc voltages to H-bridge inverters and a coupling inductance with internal resistance ($L_f + R_f$) connecting to ac grid. The output of this cell will have three levels name $+V_{dc}$, *0* and $-V_{dc}$. This circuit requires about four switching devices per phase. The circuit has many advantages like simple, modular, improved waveform which results in reduced total harmonic distortion (THD). The Cascaded Multilevel Inverter circuit provides high quality output when the number of levels in the output increases and also this reduces the filter components size and cost.

3. SYSTEM DESCRIPTION

The single line diagram representation of the system under study is shown in Figure 2. It consists of AC system of 440V, 50 Hz with source impedance of (0.625 +j0.0199 Ω). The two different loads are connected at PCC (Load 1 of 10

Ω/phase & Load 2 of 10Ω/phase, both balanced). The 3- phase symmetrical (L-L-L-G) fault is created at load1 on bus B1 where the corresponding sag occurs on bus B3. The source &load parameter are kept constant as well as the fault occurring time (0.04sec) and fault clearing time (0.16sec) with the simulation run time (0.2 sec) are kept constant throughout the system simulation. The fault impedance for system is kept constant at 3 Ω for three levels inverter based DSTATCOM. The value of coupling inductor and resistance is 6 m H, 0.5 Ω respectively. The dc link voltage of 600 V & switching frequency 4000 Hz is used for the system simulation

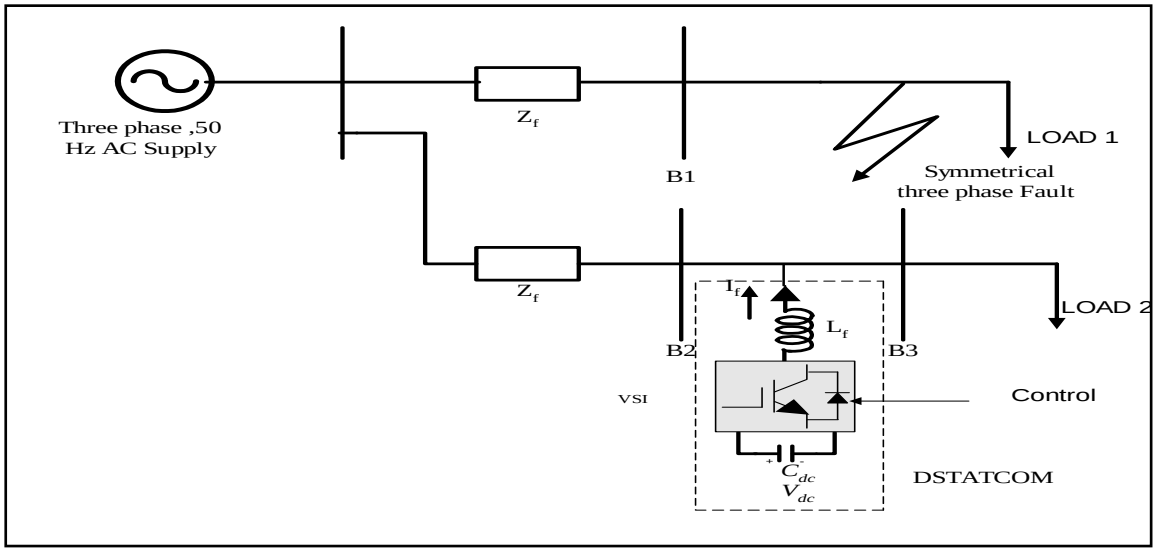


Figure 2. System Block Diagram

4. CONTROL SCHEME

The control block diagram of the cascaded three-level converter-based DSTATCOM is shown in Figure 3. The three phase source voltages (V_{sa}, V_{sb}, V_{sc}) are applied to three-phase, Phase Locked Loop (PLL) to synchronize the three-phase voltages at the converter output with the zero crossings of the fundamental component of the supply phase voltages. The PLL provides the synchronous reference angle required by the abc-dqo (and dqo-abc) transformation. The three phase cascaded inverter currents (i_{la}, i_{lb}, i_{lc}) are converted into equivalent direct axis and quadrature axis component currents (i_d, i_q).

In order to maintain the reactive power drawn from the source as zero, the output currents of the cascaded H-bridge inverter are controlled in such a way that the inverter supplies the required load reactive power. Thus for a power factor of unity at source end, the load reactive power sets the reference for inverter control which sets iq reference (i_{qref}) as l_{qload}. The reactive current supplied by the inverter (i_q) is subtracted from the reference value (i_{qref}=I_{qload}) to obtain the error in reactive current for full compensation. This error signal is passed through a PI controller block to obtain the reference voltage signal (V_{qref}), which is fed to the dqo-abc transformation block. The reference for i_d (i_{dref}) comes from the DC link voltage PI controller, which maintains the DC link voltage (V_{dc}) at reference value (V_{dcref}). The active current supplied by the source (i_d) is subtracted from the reference value (i_{dref}) and this error signal is processed through a PI controller block to obtain the reference voltage signal (V_{dref}), which goes as another input for dqo-abc transformation. PI compensators for current and voltage loops are tuned to give the optimum performance. The output voltage signals of transformation block (dqo-abc) act as reference voltages (V_a, V_b, V_c) for PWM signal generators of cascaded H-bridge converter. These signals are compared with a triangular carrier wave to obtain PWMsignals for Cascaded H-bridge inverter phases respectively.

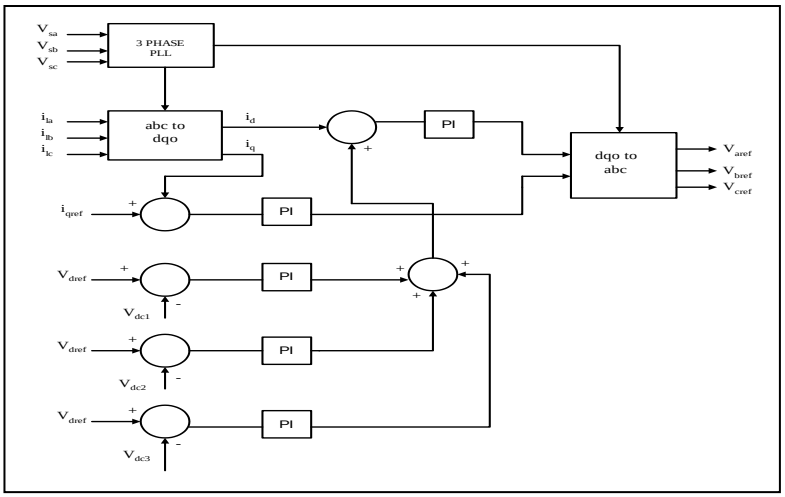


Figure 3. Control block diagram of a Cascaded H-bridge inverter based DSTATCOM

5. SIMULATION RESULTS

For the mitigation of voltage sag 3-level H-Bridge Inverter based DSTATCOM is used. For simulation purpose the fault is created at 0.04sec& clear at 0.16 sec with simulation run time 0.2 sec. The fault impedance is kept constant at 3 Ω. The fault is created at bus B1 & corresponding sag occur at bus B3.For generating the gate pulses for the H-Bridge inverter In Phase Disposition (IPD) sinusoidal pulse width modulation technique is used because IPD gives the better harmonic profile as compared to other sinusoidal pulse width modulation technique.

The switching frequency is kept at 4000 Hz. The injected three phase voltage is of 3-level while that of line voltage is 5-level as shown in Figure 4.During fault the sag magnitude at bus B3 is decreases from 1 pu to 0.6714pu with 32.86 % of sag as shown in Figure5(a). For sag mitigation DSTATCOM of 36.69 KVA with a dc link voltage of 600V is used. It is observed that DSTATCOM injects a current 100 A into the system at PCC in Figure 5 (b) & compensate the voltage at bus B3 as shown in Figure 5 (c).During sag there is a drop in active and reactive power at the bus B3 by 89% as shown in Figure5 (d) hence the DSTATCOM also compensate for the power by 75 % restoring its value close to prefault condition. The various simulated results of voltage sag mitigation using 3-level H-Bridge Inverter based DSTATCOM as shown in Figure 5(a-f)..The use of cascaded H- bridge multilevel inverter based DSTATCOM gives better result in terms of THD i.e. reduction in the harmonics. It is seen that 3-level inverter the THD is 56.67% which is less than conventional invereter.

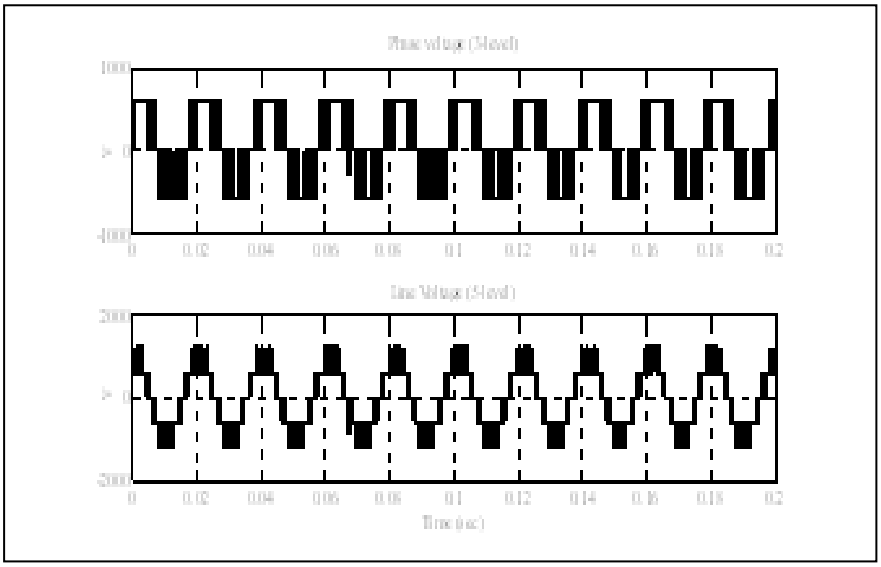
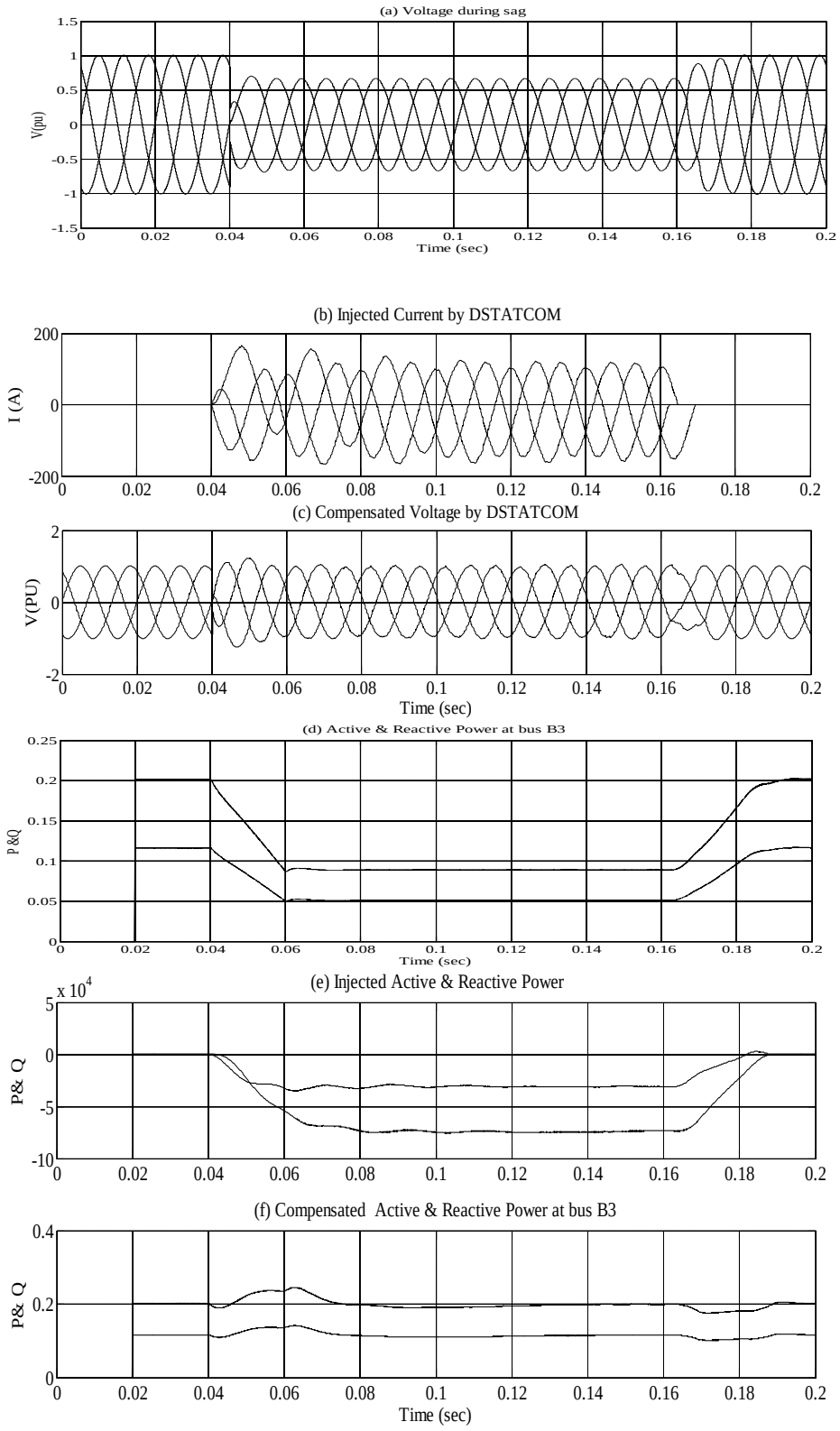


Figure 4. Phase voltage & Line voltage for 3-level inverter based DSTATCOM



& Reactive Power At Bus B3 (e) Injected Active & Reactive (f) Compensated Active & Reactive Power at bus B3 Power By DSTATCOM

6. CONCLUSION

The paper presents the principle of operation of cascaded H-bridge converter and simulation studies on cascaded converter based DSTATCOM using Sinusoidal PWM control. It is observed that the DSTATCOM is capable of supplying the reactive power demanded by the load both during steady state and transient operating conditions. Also it is more effective than conventional inverter.

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