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Synthesis of Quantum Circuit for FULL ADDER Using KHAN Gate

Madhumita Mazumder

West Bengal University of Technology, West Bengal

ABSTRACT

Reversible and Quantum logic circuits have more advantages than the common circuits, like low power consumption. To design future computers these circuits are good choice for us. In reversible logic circuit, parity preservation is very important issue. Parity Preserve of a reversible gate means, parity of inputs and outputs of the gate are equal. Reversible circuits made by these gates are also parity preserve. Quantum Gate is the primary gate level element for construction of quantum computer that perform the computation. Khan Gate (NG) is the 3*3 parity preserving reversible gate. In this work, Khan Gate is implemented using quantum gate CNOT, NOT, positive and negative controlled Toffoli gate and Swap gate. This implementation is used for construction of Full Adder quantum circuit using Quantum Representation of Khan gate Gate.

Keywords: Classical Circuit, Quantum computing, Quantum Circuit, Reversible Logic, Reversible Gates.

1. INTRODUCTION

In the last few decades advancement of the IC fabrication technology increases the counting of components IC exponentially [1]. According to Moore's law [2] this number is doubling in every 18 months. For this reason, the components size reducing to atomic level that increases the heat dissipation during computation and affects the performance of the processor. According to Landauer's Principle [3], for every bit of irreversible operation, kTlog2 joules amount of heat will be generated that goes to the computing environment. When components of IC reduce atomic level can computing process fails, then quantum physics [4] can help to continue the next generation computation. So, for future, reversible computation [3] and quantum computation [4] are most important methods. Reversible Gate [5] is the basic gate level element of reversible computing. 3*3 Khan Gate (NG) is reversible gate. This Khan Gate is implemented using quantum gates. Finally Quantum Full Adder Circuit is implemented by this Quantum representation of khan Gate.

2. BACKGROUND

2.1 Reversible Gate*:*

A gate or a circuit is called as reversible if the numbers of inputs are equal to its number of outputs (Figure 1). This is, a reversible gate performs only the permutation of its input vectors. If a reversible gate has p inputs, and therefore p outputs, then we call it a p*p reversible gate. A p*p gate is said to have width p. There is (2p)! Possible reversible gates of width p. The term Reversibility in computing implies that information about the computational states cannot be lost. So it is possible to recover any earlier stage by computing backwards or un-computing the results. This is called as logical reversibility [4], which can be gained only after employing physical reversibility. The term Physical reversibility is a process that dissipates no energy to heat. Practically perfect physical reversibility is not possible to achieve.

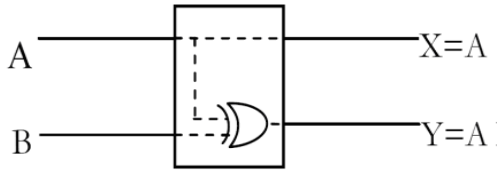

Figure 1: Reversible XOR gate

2.2 Quantum Gat:

In quantum circuit model of computation, a quantum logic gate is a basic quantum circuit, operating on a small number of qubits. They are the building blocks of quantum circuits, like as classical logic gates and are for conventional digital circuits. But classical logic gates are not reversible. However, classical computing can also be implemented by using reversible gates (Figure 2). For example, the reversible Toffoli gate can implement all Boolean functions. This gate has a direct quantum equivalent, showing that quantum circuits can perform all operations performed by classical circuits.

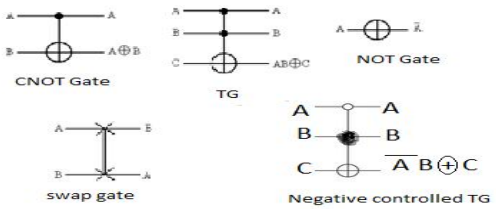

Figure 2: Quantum Gates

2.3 Classical full-adder Circuit:

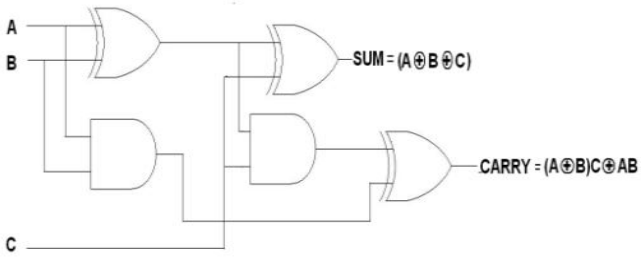

Figure 3: Classical Full Adder Circuit

2.4 Khan Gate & Full Adder Circuit:

In paper [6] Khan gate is 3*3 parity preserving Khan gate is described as shown in Figure 4. This is readily verified by comparing the input parity A B C to the output parity P Q R .The newly proposed NG gate is universal in the sense that it can be used for implementing arbitrary Boolean functions.

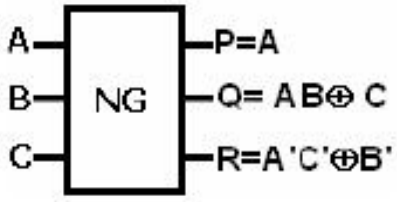

Figure 4: 3*3 Parity Preserving Reversible Khan Gate

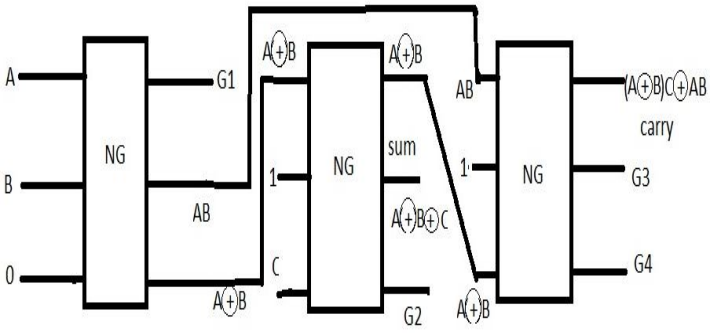

Figure 5: Fault Tolerant Proposed Full Adder Circuit Using NG

The truth table of reversible Khan gate is shown as follows in Table 1:

Table 1: Truth Table for Khan Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	1	0	0

3 PROPOSED CIRCUIT

3.1 Proposed Quantum Circuit for Khan Gate

Quantum Gate Implementation of 3*3 Khan Gate is given in Figure 6. Here, One is Garbage value; A,B,C are the INPUTs and P, Q, R are the respective OUTPUTs. One constant input is used.This proposed quantum circuit for Khan Gate is implemented with Toffoli Gate(positive and negative controlled), CNOT Gate, NOT Gate, Swap Gate.

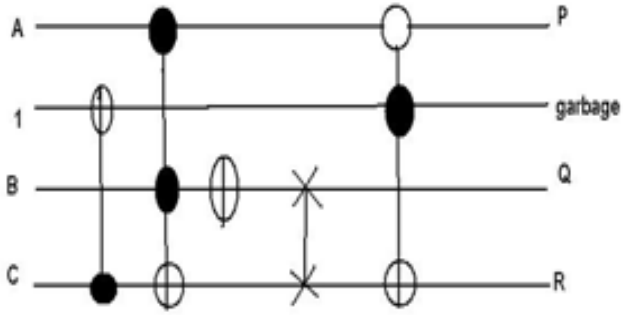

Figure 6: Proposed Quantum Circuit for Khan Gate

3.2 Proposed Quantum Circuit for Full Adder

In the previous section, established the minimum number of garbage outputs and constant inputs required to design a fault tolerant reversible full adder circuit [2] and then proposed a realization of fault tolerant reversible full adder circuit using the newly proposed parity preserving 3*3 reversible gate NG and that is efficient than the existing designs. The proposed full adder circuits is implemented by proposed Khan gate circuit and find the sum and carry. Sum is represented by 's' and carry is represented by 'c' in Figure 7.

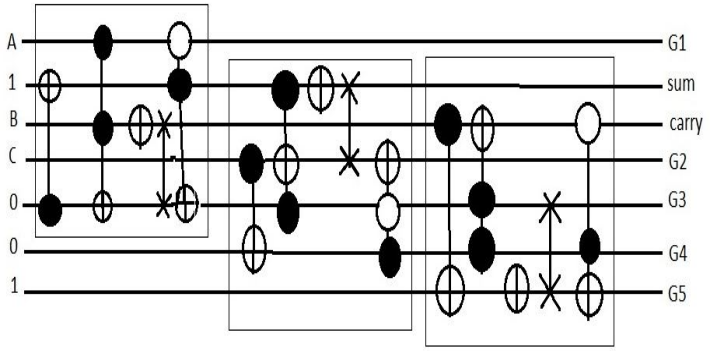

Figure 7: Proposed Quantum Circuit for Full Adder

4 SIMULATION & RESULT

These proposed quantum circuits are implemented in RCViewer+ (Version 2.31) as discussed earlier. To calculate quantum cost, the sums of the quantum costs of its gates are calculated. Quantum cost depends on no. of garbage value and no. of constant value and cost of each gate.

4.1 The proposed quantum circuit of Khan gate

Proposed Quantum Realization of 3*3 Khan Gate is represented as Figure 6. This quantum circuit for Khan Gate is implemented with positive and negative controlled Toffoli Gate, CNOT Gate, NOT Gate, Swap Gate.

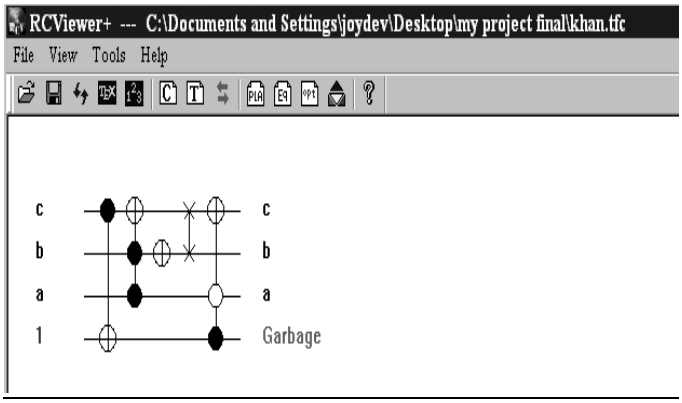

Figure 8: Proposed Quantum Circuit for Khan Gate in RC-Viewer+

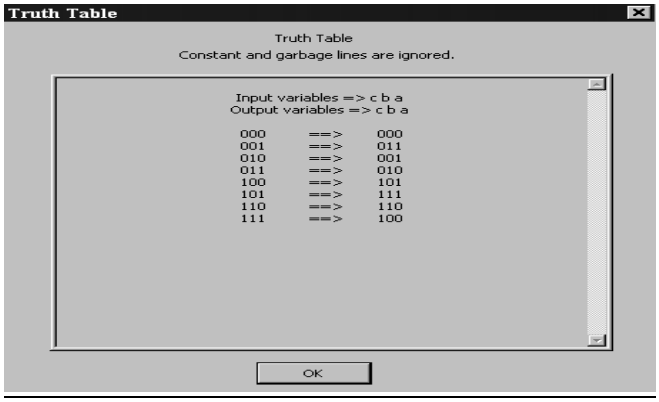

Figure 9: Truth table for proposed Khan gate

After decomposing into primitive gates, the result will be,

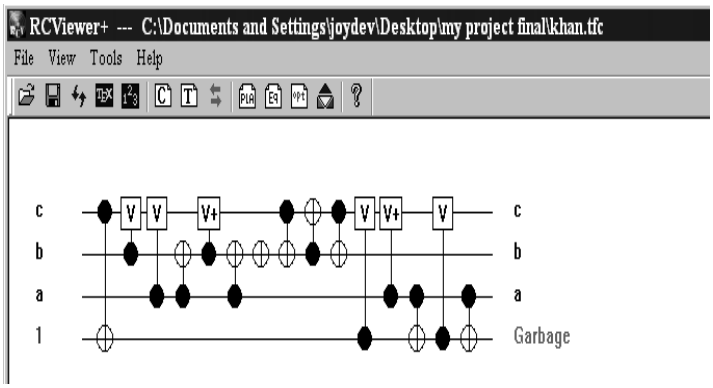

Figure 10. Decomposing proposed circuit into primitive gates

Here we use negative control TG in this proposed circuit for Khan Gate, the quantum cost will be reduced.

4.2 The Proposed quantum circuit of Full Adder circuit using proposed Khan gate

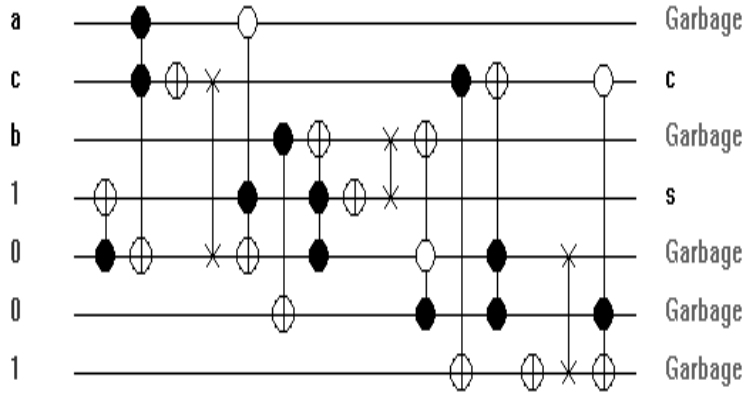

Figure 11: Proposed Full adder Quantum Circuit using Khan gate

The respective Truth Table for this Proposed Full adder circuit is shown by Fig 12. After decomposing into primitive gates, the result will be just like Fig 13.

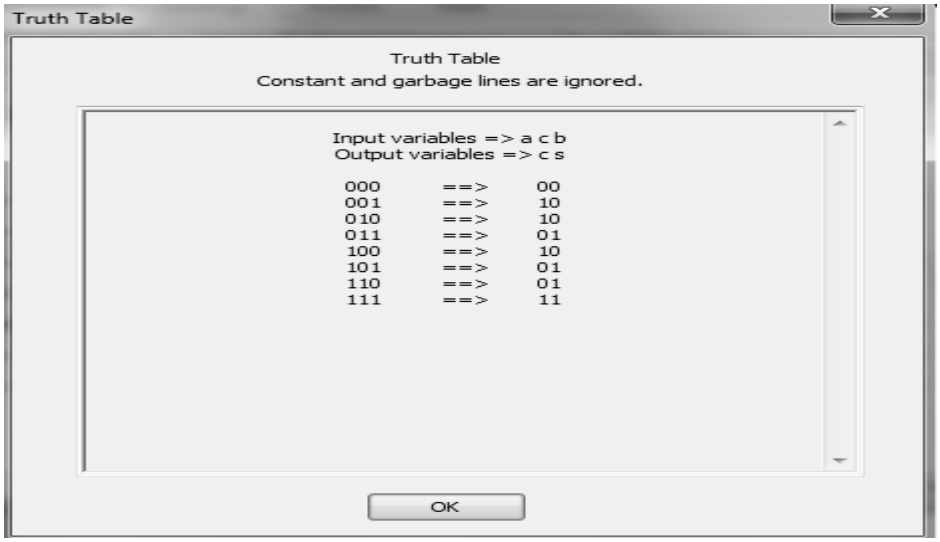

Figure 12: Truth table for proposed full adder circuit using proposed KHAN Gate

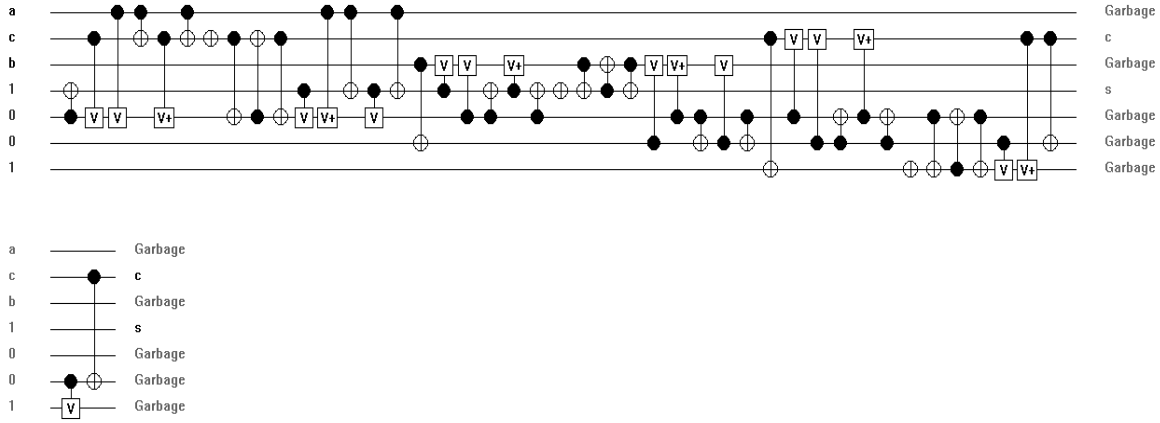

Figure 13: Decomposed Proposed Full adder circuit using Khan Gate

5 QUANTUM COST CALCULATION

Quantum Cost is the one major performance issue of the quantum circuit. The quantum cost of a circuit is the sum of the quantum costs of its gates. In this paper the quantum realization cost of NOT, CNOT ,and positive and negative controlled Toffoli gate , swap gate are considered 1,1,5,3,5 respectively. The Quantum cost for Toffoli gate with negative control is 3. According to Figure 8, we want to calculate the quantum cost for Khan gate with negative control TG(quantum cost=3),the calculation will be, (1+5+1+5+3) equals to 15 .we can also calculate the quantum cost of proposed full adder circuit like this way from figure 11 .

5.1 quantum cost of proposed circuit of Khan Gate(As shown in Figure 14)

5.2 Quantum cost of proposed quantum full adder circuit (as shown in Figure 15)

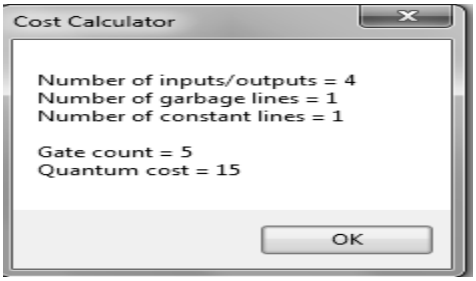

Figure 14: Quantum cost for Proposed quantum Khan gate with negative control TGs

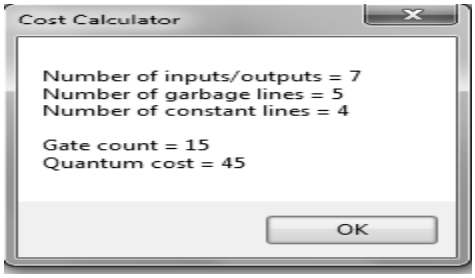

Figure 15: Quantum cost for Proposed Quantum Full Adder Circuit Using quantum Khan Gate

6 CONCLUSION

In this paper, Quantum representation of Khan Gate and Quantum full adder circuit is designed by that Khan Gate Circuit are represented by the quantum logic gates. We find out the general quantum cost from proposed Quantum Circuits.In Future we will try to reduce the quantum cost of these proposed circuits and also find an overall circuit PTM from gate matrices for evaluates the circuit reliability.

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