A DFT technique for MCM (Multi Chip Module) testing

Prof.U.W.Kaware¹, Ms. Anushri Garud² and Mr. Shubham Deshmukh³

¹Assistant professor, JDIET, Yavatmal (Maharashtra)
²Final Year student, JDIET, Yavatmal (Maharashtra)
³Final Year student, JDIET, Yavatmal (Maharashtra)

ABSTRACT

Aggressive technology scaling has been the mainstay of integrated circuit design for the past 30 years. This is posing serious challenges to integrated circuit testing and its long term reliability. A major source of failures and test escapes in the integrated circuits can be attributed to timing only parametric failures. Products motivated by performance-driven or density-driven goals often use Multi-Chip Module (MCM) technology, even though it still faces several challenges that need to be resolved before it becomes a widely adopted technology. Among its most challenging problems is achieving acceptable MCM assembly yields while maintaining quality requirements. This problem can be significantly reduced by adopting adequate MCM test strategies that is to guarantee the quality of incoming bare (unpackaged) dies prior to module assembly, to ensure the structural integrity and performance of assembled modules and to help isolate the defective parts and apply the repair process. In this paper today’s MCM test problems are described and the corresponding test and design-for-testability (DFT) strategies used for bare dies, substrates, and assembled MCMs are presented.

Keywords: MCM testing, DFT, bare dies, substrate.

1. INTRODUCTION

A design for testability (DFT) technique is geared towards the detection of such hard-to-detect defects in high performance integrated circuits. By using this technique it is expected to reduce the overall test cost, while improving the long-term reliability of high end integrated circuits. Today’s need for denser packaging technologies is mainly driven by products requiring smaller physical sizes and higher performances. The MCM (Multi chip module) technology is a key solution to meet such miniaturization and performance requirements. Contrary to the conventional packaging technology (i.e., boards populated with packaged chips), an MCM (Multi chip module) typically consists of a single package containing multiple bare dies (unpackaged chips) and discrete components. MCMs are primarily used to come up with small size products in military equipment and advanced consumer products, telecommunication equipment and high speed computers are typically performance-driven applications and often require MCMs to achieve very high speed operations. In addition to the size and performance gains, MCMs offer other advantages if compared to single die devices performing the same function. Examples of such advantages are the use of multivendor components that is to mix different process technologies (bipolar, CMOS, digital and analog, etc.), and to reduce the overall development cost and time and it is also used to achieve high density module-level interconnects. MCMs today use diverse types of chip-to-substrate attachment techniques, such as wire bond, Tape Automated Bonding (TAB), and flip-chip Mess. Co-fired ceramic (MCM-C), which basically is a hybrid circuit technology with thick film screen printing; laminates (MCM-L), which is an advanced form of printed circuit board technology and is used for midrange performance and low cost needs and MCM-D – deposited MCM. The modules are deposited on the base substrate using thin film technology. Moreover for substrate to- board attachments multiple solutions are in use some based on peripheral input/outputs and others based on surface input/outputs, such as Ball Grid Array and Land Grid Array technologies. The use of MCMs reduced the interconnect delays significantly.

2. DESIGN FOR TESTABILITY

Design for Test (“Design for Testability” or “DFT”) is a name for design techniques that add certain testability features to a microelectronic hardware product design. The premise of the added features is that they make it easier to develop and apply manufacturing tests for the designed hardware [1]. The purpose of manufacturing tests is to validate that the product hardware that contains no defects otherwise adversely affect the product’s correct functioning. The tests are applied at several steps in the hardware manufacturing flow for certain products, may also be used for hardware maintenance in the customer’s environment. The tests generally are driven by test programs that execute in Automatic Test Equipment (ATE) or, in the case of system maintenance, inside the assembled system itself. In addition to finding and indicating the presence of defects (i.e. if the test fails), tests may be able to log diagnostic information about the
nature of the encountered test fails. This information can be used to locate the source of the failure. In other words, the response of patterns from a good circuit is compared with the response of using same patterns from a DUT (device under test). If the response is the same or matches, the circuit is good else the circuit is faulty. DFT plays an important role in the development of test programs and for test application and diagnostics. Automatic test pattern generation (ATPG) is much easier if appropriate DFT rules and suggestions have implemented. The common understanding of DFT in the context of Electronic Design Automation (EDA) for modern microelectronics is shaped to a large extent by the capabilities of commercial DFT software tools as well as by the expertise and experience of a professional community of DFT engineers researching, developing, and using such tools [1]. DFT is a design process intended to achieve a high level of testability by incorporation, early in design phase of following circuit, module, equipment, system characteristics:

- Initialization: The ability to initialize a system with external stimuli to the operating characteristics of the system. For digital systems this includes being able to disable internal clocks.
- Controllability: The ability to control the functions of the systems with external test stimuli, including clocks and ability to break up chains and feedback loops.
- Observability: The ability to observe the functions of the systems through adequate test points (0-100%) using integrated diagnostics (i.e BIT, ATE etc.)
- Accessibility: The ability to have (0-100%) access to units internal part structure and partitions, depending on mission requirements and limited test points placement.

The means by which DFT is implemented will require the ability to analyze the above characteristics for a given system to identify where improvements are necessary to provide adequate initialization, controllability, observability and accessibility. There are several tools and methods available to the analyst that will provide the necessary information needed to implement DFT techniques.

2.1 DFT Objectives

From definition of DFT, the goals and objectives of any DFT program are to minimize the costs associated with testing for equipments malfunctions while maximizing system gain. More specifically these objectives are met by using DFT technique to help determine where functional test and condition monitoring are needed to assure gain requirements and what strategies are needed to maximize malfunction detection and isolation and decrease test times. In meeting DFT objectives the benefits of lower test program set (TPS) development cost and lower system life cycle support costs will more than out weight the cost of implementation.

2.2 DFT methods

2.2.1 Ad-HOC DFT method

Ad-hoc is a special route for DFT. The ad-hoc DFT realizes on good design practices learned from experience. Some of these are:

- Avoid synchronous logic feedback: A feedback in the combinational logic can give rise to oscillation for certain output. This makes the circuit difficult to verify and impossible to generate tests for by automatic programs. This is because test generation algorithms are only known for cyclic combinational circuits.
- Make flip flop initializable: This is easily done by supplying clear and reset signals that are controllable from primary input.
- Avoid gates with larger number of fan-in signals: Larger fan in makes the input of gate difficult to observe and make the gate output difficult to control.
- Provide test control for difficult to control signal: Signals such as these produced by long counters require many clock cycles to control and hence increase the length of test sequence. Long test sequences are harder to generate. These and many other similar situations cause poor controllability and observability of signals and usually result in long test sequence and low fault coverage.

2.2.2 Structured DFT method

A structured Design for Test (DFT) methodology that was formulated for a major system design project equipments. This method includes fill scan for chip test, and an optimized boundary scan for board test. This methodology has also minimized timing degradation of the designs through intelligent scan synthesis. A structured method includes scan, partial scan, BIST that is (Built in self test), boundary scan. Out of all these methods BIST method is most significantly used for delay fault testing.

a. Scan

A scan method attempts to control and observe the internal signals of a circuit using only a small number of test points. A scan-path method considers any digital circuit to be a collection of flip-flops or other storage element interconnected by combinational logic, and is concerned with controlling and observing the state of the storage elements. It does this by providing two operating modes: a normal mode, and a scan mode in which all of the storage elements are reorganized into a giant shift register. In scan mode, the state of the circuits and storage elements can be read out by n shifts and a new state can be loaded at the same time. Scan-path design is mostly used often in custom VLSI and ASIC design, because of the impossibility of providing a large number of conventional test points.
b. Partial scan

In partial scan method a subset of storage elements that are converted into scan cells and sequential Automatic test pattern generator is typically used for test generation. Partial scan a functional portioning approach. In this a circuit is composed of a data path portion and a control portion. Storage elements on the data path are left out of the scan cell replacement process and storage elements on the control path can be replaced with scan cells. A balanced partial-scan design approach uses a target sequential depth to simply the test generation process for the pipelined or feed-forward partial-scan design. This reduces silicon area overhead and reduces performance degradation. Also it can result in lower fault coverage longer test generation time offers less support for debug, diagnosis and failure analysis.

c. BIST (Built in self-test)

Built-in self-test (BIST) is an advanced method for testing digital IC. This method requires no external equipment for test application and testing can be performed at the manufacturing stage and also at every power-up or even during normal operation. This technique permits IC chips to test themselves by embedding both test pattern generator (TPG) and output response analyzer (ORA) inside the chip. At the cost of approximate by 20% – 30% overhead in the chip area and a small performance due to additional BIST hardware, the IC chip can now perform testing through internal scan chains without an external automatic testing equipment (ATE). BIST techniques make testing of a digital IC chip easier, faster, more efficient and less costly.

d. Boundary scan

Boundary scan is a method for testing wire interconnections between individual ICs of a circuit board. This method can be used to isolate an IC chip from other chips on the board, supply desired test patterns as input and obtain output from the IC for analysis. Boundary scan is a method for testing interconnections on printed circuit boards or sub-blocks inside an integrated circuit. Boundary scan is widely used as a debugging method to watch integrated circuit pin states, to measure voltage, or to analyze sub-blocks inside an integrated circuit. The boundary scan architecture provides a means to test interconnections without using physical test probes, this involves the addition of at least one test cell that is connected to each pin of the device and that can selectively override the functionality of that pin. The combination of BIST and boundary scan methods can be used to analyze testing in multi chip modules.

3. MULTI CHIP MODULE (MCM)

A multi-chip module (MCM) is a specialized electronic package where multiple integrated circuits (ICs), semiconductor dies or other discrete components are packaged onto a unifying substrate, facilitating their use as a single component (as though a larger IC) [2]. The MCM itself referred as a chip in designs, thus illustrating its integrated nature. Multi-Chip Modules come in a variety of forms depending on the complexity and development philosophies of their designers. These can range from using pre-packaged ICs on a small printed circuit board (PCB) meant to minimize the package footprint of an existing chip package to fully custom chip packages integrating many chip dies on a High Density Interconnection (HDI) substrate. Multi-Chip Module packaging is an important part of modern electronic miniaturization and micro-electronic systems. MCMs are classified according to the technology used to create the HDI (High Density Interconnection) substrate [2]. They are as follows:

- **MCM-L** – Laminated MCM. In this the substrate is a multi-layer laminated PCB (Printed circuit board).
- **MCM-D** – Deposited MCM. In this the modules are deposited on the base substrate using thin film technology.
- **MCM-C** – Ceramic substrate MCMs. This is basically a hybrid circuit technology with thick film screen printing.

![Figure 1 A typical BIST controller](image-url)
A relatively new development in MCM technology is the so-called "chip-stack" package. Certain ICs, memories in particular, have very similar or identical pin outs when used multiple times within systems. A carefully designed substrate can allow these dies to be stacked in a vertical configuration making the resultant MCM’s footprint much smaller (at the cost of a thicker or taller chip). Since area is more often at a premium in miniature electronics designs, the chip-stack is an attractive option in many applications such as cell phones and personal digital assistants (PDAs). After a thinning process, as many as ten dies can be stacked to create a high capacity SD memory card.

Figure 2. MCM containing four bare dies

There is hardly any standardization in the MCM technology, and the MCM manufacturers often use proprietary techniques, the current issues with MCM technology are common among most existing manufacturers. Some of the important common ones are:

- The unsatisfiable quality of unpackaged chips (bare dies)
- The unavailability of their simulation models,
- The low yield of MCM assembly
- The high cost of MCM manufacturing
- The complexity of the rework process by which defective components can be diagnosed and replaced.

3.1 MCM tests and diagnostics:
The issues of bare die quality, low assembly yield, and defective component identification are, in fact, test and diagnosis problems. They are caused due to the limitations of conventional techniques used in chip and board testing. For instance, the conventional test of unpackaged chips as performed by most IC suppliers today consists of a simple parametric test and a low speed functional test at the wafer level to verify if a chip is alive. Such a test is typically below the quality level required for bare dies because it does not contain the performance and reliability tests. In general, after its assembly onto the MCM substrate if a bare die is found defective, either the MCM is repaired by removing the bad chip and replacing it with a presumably good one or the whole substrate is scrapped with the rest of the chips. Both alternatives are often expensive and undesirable. Hence, test strategies that result in providing bare dies with high quality prior to mounting them onto the MCM substrates are necessary[3]. Another problem appears during the test of assembled MCMs, if conventional board testing is used for MCMs. Here the in-circuit testing, it faces two major obstacles. One is the difficulty of accessing internal nodes in an MCM, due to high chip density and small interconnections. The other is due to the speed limitations of automatic test equipment used for boards. Hence, it is difficult to diagnose and to apply performance test at the MCM level. The MCM manufacturing process requires isolating the defective components. Hence, the module level test approach needs to provide diagnostic capabilities during the MCM repair process. The MCM production flow can be divided into four major non-overlapping processes, as shown in Figure 3. They are the process of fabricating the wafer, the production of individual bare dies; the fabrication of substrates; and the assembly of bare dies and substrates to compose MCMs. Testing takes place during each one of these four processes. The test related activities are represented by shaded boxes in Figure 3. They can be divided into four sets of activities that correspond to the MCM production processes. They are: wafer test, bare die test,
substrate test and assembled module test and rework. Each of these test processes faces certain challenges and requires the adoption of specific strategies to meet the MCM quality requirements and improve its yield.

3.2 Issues of testing unpackaged chips

3.2.1 Wafer and bare die testing

Chip-level testing is done by chip manufacturers in two stages. First, at wafer level, they typically perform a wafer sort on the unpackaged chips. This consists of running a structural integrity test (functional test) using ATPG patterns at low speed and an input/output parametric test. The second stage takes place after the chip is packaged. This consists of a comprehensive performance and reliability test. In MCMs as bare dies are attached directly to a substrate, therefore the complete set of tests, as in the mentioned two stages, need to be performed on unpackaged chips. This means that, the test performed on bare dies has to include the performance and reliability tests, which are conventionally done during the second stage (i.e., at the packaged chip level). The low speed structural integrity and input/output parametric tests for bare dies are performed at the wafer level test. The input/output parametric test verifies that finished dies meet input/output voltage and leakage specifications. The use of regular wafer probes for this test has been a standard procedure. It is desirable to raise this coverage for packaged chips in order to improve the yield of IC production, but improving fault coverage is far more important for bare dies. The MCM yield is a composite function of the individual yields of the bare dies it contains. This can hardly be obtained for today’s complex chips if a structured testability technique such as scan or BIST is not used during the design cycle of a chip. If the chip will be packaged in an MCM, this will be one of the major changes over the conventional chip design process [4]. A performance test is used to detect delay type faults which are not included during the conventional low speed wafer level test. Bare dies often need to be tested for such faults prior to MCM assembly. If an MCM application is density-driven rather than performance-driven, performance testing of dies may not be as crucial. For performance-driven applications, at-speed testing of dies is necessary. A different approach to this problem is packaging samples from each wafer lot and testing the samples for performance, based on the fact that an individual wafer has a maximum spread of only a few percent. However, this approach cannot be adopted for critical MCM applications in terms of performance. Another solution would be to mount the bare die in a (permanent) carrier and apply the performance test on it. A number of carrier based solutions have been proposed recently. Another solution would be to invoke a built-in at-speed test in the bare die[4]. This
requires a minimal improvement in the high speed capabilities of existing tester probes. The complexity of bare die testing differs from one attachment method to the other. The flip-chip attach, where the die bond pads are distributed all over the active area of the die, and the wire-bonded dies cannot be effectively tested at-speed by conventional test techniques until the assembly. On the other hand, the dies designed for TAB (Tape Automated Bonding) attachment can be tested for performance, after inner lead bonding, by conventional test techniques before entering the assembly process. Hence, the defective TAB dies can be removed or repaired prior to assembly. This will increase MCM test yields. TAB devices are poor and expensive. Devices that are designed for TAB and wire-bond attachment are more difficult to replace than flip-chip devices. The major drawback of flip-chip is the difficulty of applying performance testing. Chip-level reliability test using burn-in is another major reason to use carriers. Chips are detected using burn in test if they have infant mortality. Burn-in is usually done on packaged dies, and also be performed on TAB dies. The wafer testing for MCM bare dies face three major difficulties: the first is the expected known good die quality which necessitates test vector sets with very high fault coverages, the second is the speed limitations of existing wafer probes, and hence the problem with performance testing and the third is the problem of burn-in associated with the required reliability testing.

3.2.2 Substrate testing
It is important to test the substrates for electrical integrity that are prior to attaching the dies. A substrate defect hurts MCM yield as much as, or more than, poor yielding die. Substrate repair is sometimes not possible and components are often damaged during the removal process. Hence, detection of a substrate defect can be extremely expensive. Typically, substrate testing failure types include opens and shorts. Substrate testing is done either by flying probes, such as two moving probes using resistance, or a single moving probe measuring the capacitance of each node. Mechanical probes are slow for substrates with a large number of nodes. They may damage the substrate and have serious problems with dense package geometries. Contactless probing, such as electron beam probing, is much faster than mechanical probing. Voltage Contrast Electron-Beam test is an attractive technique for high-throughput contactless testing of unpopulated packaging substrates [4]. Results have shown that it is possible to effectively test today’s MCM substrates with the existing mechanical probing or contactless probing techniques.

3.2.3 Issues in testing Assembled MCMs
Testing assembled MCMs combines the complexities of testing individual chip and testing printed circuit boards. The role of assembled MCM test is to ensure that all the individual dies are properly connected to the substrate and are still maintaining their structural integrity and that the assembled MCM, as a single device, meets its performance specifications. This requires the following three tests respectively:

a. Interconnect Test.
An interconnect test, it is used to detect and identify intra-die assembly defects. This type of test is systematically performed in conventional board testing. As the density of MCM substrates is more, different micro-probing solutions have been introduced for module levels interconnect testing. If an MCM substrate has very limited accessibility, then the advanced micro probing techniques cannot be used in it. In such cases, it is necessary to incorporate testability features in the substrate design and the design of individual chips.

b. Structural Integrity Test.
A full functional test at the module level for each die is used to detect its structural integrity. As the chips there are protected by their individual packages this type of test is not typically used in board testing, whereas in MCMs, the bare dies have the possibility of being damaged during the process of handling and mounting. In addition, thermal stresses which are present while the module is powered. This can result in damages to the individual dies [5]. Hence, we need to run a whole functional test, similar to the one applied at the die level, after the dies are mounted on a substrate. One possible way to handle this at the module level is by applying the functional test sets of individual dies. This is possible only if there is direct accessibility to the input/outputs of each die. In the case of dense substrates, such accessibility is not possible, hence a new functional test sets need to be developed and applied on the entire module, or the test sets need to be embedded in the individual dies, such as in Built-In Self- Test. In module level functional test, the test set need to provide detection of structural integrity of individual dies and identification of defected dies. These test sets are developed by the MCM designer using module level simulation if the behavioral models of the individual dies are available. The development of such a test set is possible for MCMs with small number of dies, but it becomes extremely difficult for complex MCMs. In such cases, the design for testability (DFT) oriented Built-In Self-Test solution is the choice.

c. MCM Performance Test
As MCMs are often used for applications requiring high performance, a performance test for the entire module is necessary. The MCM performance test is an at-speed test on the assembled MCM. It tests for propagation delay times that are path delays, including chip delays and substrate routing delays. The above two tests (i.e., interconnect test and die structural integrity test) cannot test the entire module performance. The performance test can be very short since thorough performance detection is applied to each die. This test often requires automatic test equipment with high pin count and high speed capabilities, which are expensive. As shown in Figure 3, the repair cycle sometimes includes cap removal, if the repair is performed after the final test and rework [5]. The cost effectiveness of repair depends on the
MCMM under test. For instance, a failed MCM made on laminate-type substrate may be scrapped because of its relatively low cost. In general, an MCM test procedure can be followed by a diagnostic procedure in order to identify the defective element in the MCM and hence allow for adequate repair.

4. DESIGN FOR TESTABILITY FOR ASSEMBLED MCMs

Design for testability strategies are used to create the necessary accessibility in such cases. The ideal DFT approach for MCMs is based on implementing chip level BIST and module level Boundary-Scan in the MCM design [6]. Both BIST and Boundary-Scan are testability techniques, are meant to improve the controllability and observability of a circuit under design to make it testable. BIST is the capability that allows a circuit to test itself. The BIST schemes that are used in MCMs are the ones that provide very high fault coverage. Most of these schemes run at system speed and typically achieve the required fault coverages. Boundary-Scan is a general DFT strategy. The architecture of Boundary-Scan allows associating memory cells with each input and output of every die so that predetermined signals can be sent across the interconnections and be captured for observation. The Boundary-Scan architecture provides a single Test Access Port (TAP) to each chip, through which all the test related instructions and data can be transferred. BIST is also executing through the Boundary-Scan TAP. The incorporation of BIST and Boundary-Scan in a chip design and techniques to obtain very high fault coverages at the chip and the module levels are covered in and respectively.

4.1 Integrity and Identity Check.

This test is used to verify the integrity of Boundary-Scan circuitry. The Boundary-Scan standard provides a certain method to perform this test, which provides relevant diagnostic information regarding the location of the failure if any. A test to check the identity of each die is performed by following integrity test. The Boundary-Scan standard allows permanent storage of chip level ID codes. Each MCM die will have its ID code, which is read through the Boundary-Scan TAP and is compared with a reference value. This test detects if a wrong die is mounted on the substrate, or a die is not oriented properly. This is especially important with MCMs since many of the chips on an MCM tend to be manufactured from the same die footprint [6]. Hence, it is almost impossible to rely on visual inspection. The output of this test carries diagnostic information, which is used to identify the wrong or incorrectly oriented dies.

4.2 Interconnect Test

This test is meant for checking proper interconnection of dies with the substrate. The existence of Boundary-Scan chain in the module, consisting of the Boundary-Scan registers of each die and the connections between these registers through the substrate, creates a virtual electronic bed-of-nails built into the module. This bed-of-nails is independent of the module’s density [7]. Boundary-Scan latches can sense across all interconnects. This permits testing the opens or shorts between inputs/outputs of two dies, and between inputs/outputs of a die and the inputs/outputs of MCM. The Boundary-Scan based interconnect tests provides diagnostic information identifying the faulty net and the type of fault. This information is useful for the repair process.

4.3 Functional Chip Test

This operation is chip level BIST run and is similar to the one performed during the bare die test using BIST. It is considered necessary to be repeated in order to detect the failures that may have occurred during the handling and mounting processes of bare dies. The test patterns in this operation are generated there is no need to access each pin in order to run the functional test. The only access needed is to the TAP of each die, and that is possible through the Boundary-Scan chain of the MCM. Since nearly all MCM users must rely on outside suppliers for dies, substrates, and interconnection related components, and since information may need to pass through several companies before reaching the final MCM assembler, BIST is considered a very advantageous test approach. It is a built-in capability, and is transparent to such transfers. And it also provides diagnostic information. The analysis or automatic comparison of the BIST responses can identify which chip has failed. However, the benefits of using BIST seem to dominate. Today, various chip suppliers are using BIST in their manufacturing test. Those suppliers need to provide information, to MCM manufacturers who are using their chips, regarding the BIST execution and its fault coverage. This will allow the usage of existing BIST capabilities during MCM assembly test.

4.4 Performance Test

The MCM performance test is meant to verify its performance requirements, i.e., all the chips on an MCM substrate can properly communicate with each other. A performance test detects propagation delays that include die delays and substrate delays. The speed limitation of today's automatic test equipment often prevents MCM manufacturers of testing the whole module at its system speed. The chip level BIST and Boundary-Scan techniques do not provide a performance test for the entire MCM. Because the Boundary-Scan based interconnect test is a slow speed structural test and the chip level BIST is an at-speed structural test, but only for inter-chip (occurred in individual chips) faults. Hence, a DFT-based solution such as the multi-chip BIST scheme is used to test the whole module for performance of module. In addition to their detection, MCM performance faults need to be located too. The availability of Boundary-Scan architecture in individual dies is useful in this case too, since the Boundary-Scan sample mode can be used to take snapshots. With BIST and Boundary-Scan incorporated into the chip designs, the testability facilities necessary to run the above four stage procedure are ready for the module level test.
5. CONCLUSION

In this paper, a design for testability and how MCMs are tested using DFT techniques is explained. With the help of this technique it is possible to detect a large range of delay faults compared to non-DFT technique. It is expected that this technique will help in moving fault detection and ensuring long term reliability of high and digital IC’s. Given diversity in today’s MCM technology, numerous test strategies are used. This paper presents MCM techniques and its implications on MCM testing strategies. Here the challenging problems in MCM test and number of currently available test solutions are explained and reviewed. Some of present strategies are based on external test resources only and other combined embedded solutions such as BIST and Boundary scan with external test.

References


AUTHOR

Prof. U.W. Kaware received his ME in Digital Electronics from Sant Gadgebaba Amravati University. He is an assistant professor in Electornics and Telecommunication Department at Jawaharlal Darda Institute of Engineering and Technology, Yavatmal. He is pursuing Ph.D from Sant Gadgebaba Amravati University and his area of research is video compression.

Ms. Anushri Garud born in Yavatmal, Maharashtra in 1994. She is pursuing Bachelor degree in Electronics and Telecommunication engineering from Jawaharlal Darda Institute of Engineering and Technology, Yavatmal.

Mr. Shubham Deshmukh born in Amravati, Maharashtra in 1994. He is pursuing Bachelor degree in Electronics and Telecommunication engineering from Jawaharlal Darda Institute of Engineering and Technology, Yavatmal.