

# Delay analyzing circuit design for timing recovery

Jyotika Singh

Student BE Hons. ECE, Birla Institute of Technology and Science, Pilani, Dubai

## ABSTRACT

*For the process of recovering timing information at the receiver end of a communication channel, we use phase detectors as a part of the process. The phase detectors that exist are insensitive to a delay between timing and message signal more than 50% of the clock duty cycle. Such delay analysis is discussed and a circuit design is proposed to counteract the problem along with analysis of the drawbacks and conclusions.*

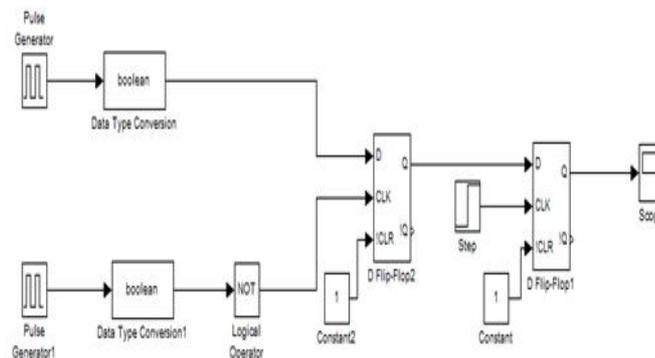
**Key words:** Clock, delay, duty cycle, phase, timing.

## 1. INTRODUCTION

Data can be sent with or without timing information. [1] Regardless, timing information is required at the receiver end to correctly receive and analyze the data that was sent. Clock or timing is used as a reference to sample the data. The clock used to do this at the transmitter end needs to be used as the receiver end as well for correct interpretation of the message sent. Phase detectors are used to detect phase differences between recovered clock and data. [1] These phase detectors cannot detect phase differences beyond  $\pm 0.5$  seconds, assuming a clock period of 1 second. [1] However, it is assumed in some scenarios that the phase difference will not be as bad as a value greater than 50% of the clock period duration, which is why these designs are justified. However, situation might not be as smooth and the sent message can be misinterpreted if the phase difference exceeds beyond a certain point. For the above stated reason, one should be aware of how much the phase difference is in terms of more or lesser than the assumed maximum detectable limit.

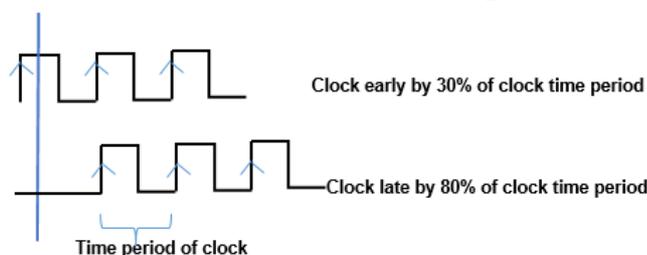
## 2. CIRCUIT AND LOGIC

In case we expect the clock to have a possible delay of more than 50% of the time period of the clock, using any of the existing designs for this determination does not give us the desired results. Putting in some thought to this, I have come up with a design for this determination. The circuit diagram for this design can be seen in figure 1. This circuit consists of two D flip-flops and one step input.



**Figure 1:** MATLAB Simulink diagram for analyzing delay implementation

Since the only difference between the clock of an early signal (less than -50% of clock duty cycle delay) and that a late clock (more than 50% of the clock duty cycle delay) is only the way the clock behaves initially, to determine the initial portion can possibly give us the desired results. This is illustrates below in figure 2.



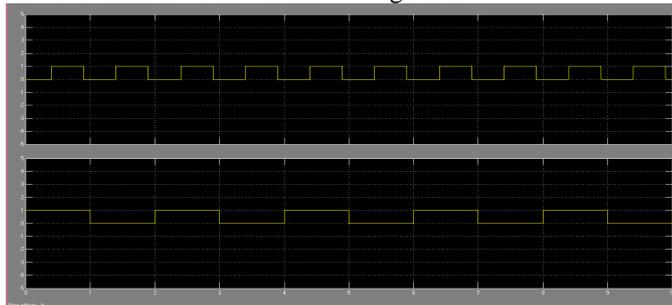
**Figure 2:** Clock early – late timing diagram

The logic behind this circuit is testing the initial difference in the portion between the two cases as seen in figure 2.aving one output of the delay case, whether the delay is greater than or less than 50% of time period of clock, and another output for clock early case, could lead to distinguish between delay and early clock scenario.

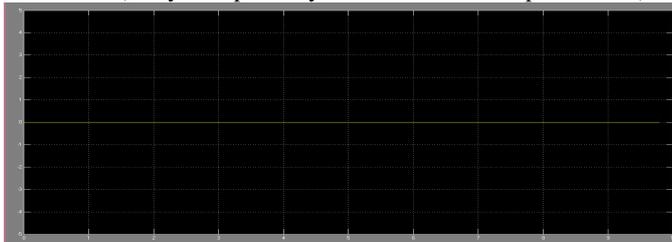
### 3. SIMULATION RESULT

The simulations for this circuit is can be seen in the following figures.

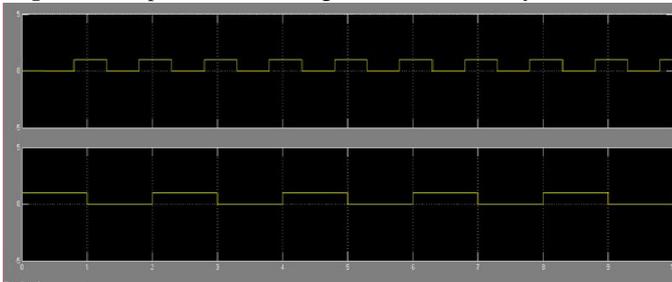
[2] Firstly, phase detectors can be used to determine the condition. In case one is uncertain about how much delay can be present between the phase of the data and the clock signal, whether it is too early or too late, the circuit shown in figure 1 would hold good to determine the condition properly. When the clock is late by 0.4 seconds, given the clock time period for one cycle is 1 second, the output is shown in figure 4. Before that, we see out clock signal delayed by 0.4 seconds in figure 3 along with our data. [1] For simplicity of analysis, we pass the preamble bits of continuous transition between 1 and 0 as the data. The clock passes through an inverter NOT gate and then goes into the circuitry that follows in figure 1. When the clock is late by 0.8 seconds, given the clock time period for one cycle is 1 second, the output is shown in figure 6. The clock and data can be seen in figure 5. This clock and data passes though the circuitry in figure 1 and leads to the respective output. When the clock is early by 0.3 seconds, given the clock time period for one cycle is 1 second, the output is as shown in figure 8. The clock and data for it can be seen in figure 7.



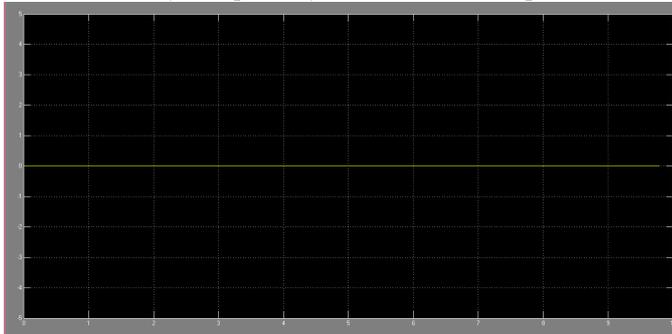
**Figure 3:** Clock (delayed in phase by 0.4 seconds with respect to data) and data



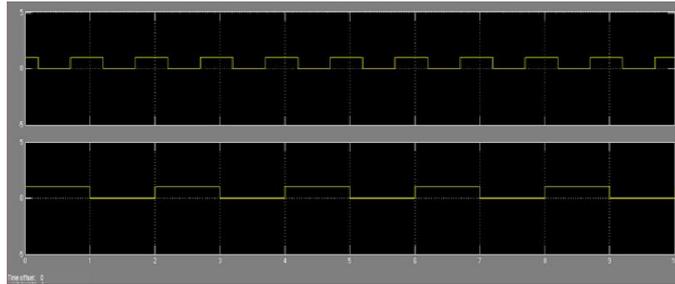
**Figure 4:** Output of circuit in figure 1 for clock delay of 0.4 seconds



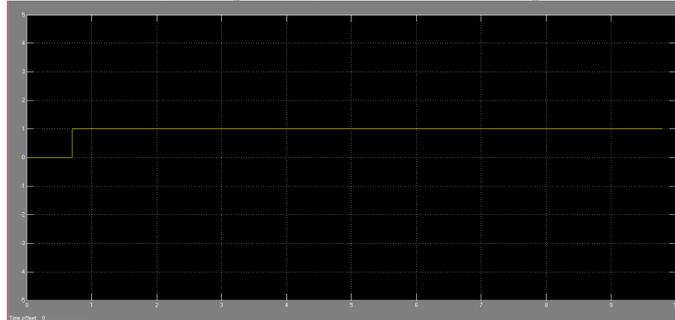
**Figure 5:** Clock (delayed in phase by 0.8 seconds with respect to data) and data



**Figure 6:** Output of circuit in figure 1 for clock delay of 0.8 seconds



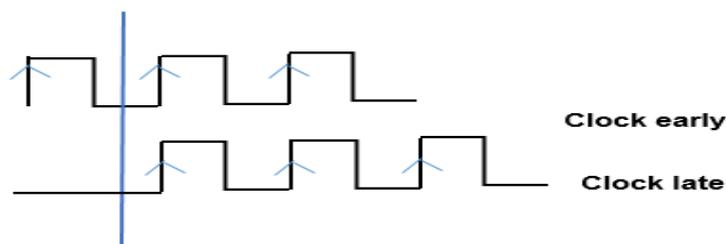
**Figure 7:** Clock (delayed in phase by -0.3 seconds with respect to data) and data



**Figure 8:** Output of circuit in figure 1 for clock early by 0.3 seconds

#### 4.. CONCLUSION

As we can see in the simulation figures, the output of the circuit distinguishes between a delay of greater than 50% of one clock cycle time period and an advancement of the clock with respect to the data of less than 50% of one clock cycle time period. The output of the circuit designed and shown in figure 1 is 0 in case the delay case is sensed to be true and an output 1 is generated if the clock early case is true. Moreover, the circuit produces an output of 1 when the clock is delayed in phase by any positive value amount. The limitation of this circuit is that it does not work for the case where the clock is early by a period greater than 50% of clock time period of one cycle. Therefore distinguishing between that and the situation where clock is late by less than 50% of the clock cycle time period does not produce results directly. In these two cases, from where the observation window starts, we see that there is no difference in the clock. This can be seen in the figure 6. The solution I propose for the above limitation is to delay the clock further by 50% of the clock cycle time, so that a difference is introduced in the starting period of the clock and therefore, a difference can be determined in case circuit in figure 1 does not give distinct result directly. Therefore this delay can be introduced for testing followed by circuit designed in figure 1.



**Figure 9:** Clock early-late timing diagram

#### REFERENCES

- [1.] Jyotika Singh, T.G Thomas, Alternative Phase Detectors for Clock Recovery at the Receiver, Birla Institute of Technology and Science, Pilani, Dubai, July 2014.
- [2.] J.D.H. Alexander. Clock recovery from random binary signals, University of Aberdeen, Scotland, September 1975.
- [3.] Hae Chang Lee. An estimation approach to clock and data recovery, thesis, November 2006
- [4.] Philipus Oh, Win Chaivipas, Akira Matsuzawa. A Study on Full Digital Clock Data Recovery (CDR), Tokyo Institute of Technology Graduate School of Science and Engineering, Department of Physical Electronics, Matsuzawa Laboratory.
- [5.] Sam Palermo, ECEN689: Special Topics in High-Speed Links Circuits and Systems, Lecture 30: CDRs, Analog & Mixed-Signal Center, Texas A&M University, Spring 2010.
- [6.] Lecture 200- Clock and Data Recovery Circuits, Georgia Institute of Technology, Summer 2003