

Design of Enhanced Hybrid Flip-Flop with Embedded Logic Module

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ABSTRACT

In this paper we propose a new kind of flip-flop which overcomes the disadvantages of static and dynamic flip-flop. We introduce a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) based on DDFF. The proposed designs eliminate the large capacitance present in the pre-charge node of several state-of-the-art designs by following a split dynamic node structure to separately drive the output pull-up and pull down transistors. The aim of the DDFF-ELM is to reduce pipeline overhead. It presents an area, power, and speed efficient method to incorporate complex logic functions into the flip-flop. The performance comparisons made in a TSMC025.

Keywords:- DDFF, DDFF-ELM.

1. INTRADUCTION

The continual push for higher clock rates and higher performance has led microprocessor designers in recent years to build super pipelined machines with multiple functional units that can execute operations concurrently. High clock rates in these machines are often achieved with fine granularity pipelining, for which there are relatively few levels of logic per pipeline stage. One direct consequence of this design trend is that the pipeline overhead is becoming more significant. This pipeline overhead is primarily due to the latency of the flip-flop or latch used and the clock skew of the system. While the clock skew varies and in some cases can be used constructively (e.g., routing the clock in the same direction of the data), the latency of the flip-flops cannot be hidden. As an example, assuming that a Flip-flop latency is three gate delays and that the clock cycle in a state-of-the-art, high-speed microprocessor is 20 gate delays, the flip-flop overhead amounts to 15% of the cycle time. This is a substantial penalty that degrades the overall performance of the system, since no useful logic operation is performed on the data when it is being latched. Another consequence of the aforementioned trend is that the number of flip-flops in the system has increased dramatically. From a few thousand flip-flops in early designs, several tens of thousands of flip-flops is not an uncommon number in current designs. Speed, area, and power are well balanced, is of fundamental importance Additional up demands a lower pipeline overhead. This overhead is that the latency related to the pipeline elements, like the flip-flops and latches. Intensive work has been dedicated to improve the performance of the flip-flops within the past few decades. Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes. There are basically four main types of latches and flip-flops: SR, D, JK, and T. the major differences in these flip-flop types are the number of inputs they have and how they change state. For each type, there are also different variations that enhance their Operations. The D Flip-Flop Latches are often called level sensitive because their output follows their inputs as long as they are enabled. They are transparent during this entire time when the enable signal is asserted. There are situations when it is more useful to have the output change only at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. Thus, we can have all changes synchronized to the rising or falling edge of the clock. There have been many methods proposed to eliminate the drawback of power consumption and latency. Due to rise in the system requirements and advanced cmos technology and speed of operation many research works has been made to increase the performance of the Flip-Flops are made. In last few years many Flip-Flops has been made to improve performance. In this paper we show the Static Flip-Flop which efficient among all Power PC and we shows how a dynamic Flip-Flop will works from these two we show Hybrid Flip-Flop which has properties of both static and dynamic Flip-Flop Hybrid latch flip-flop (HLFF) and semi dynamic flip-flop (SDFF) are considered as the classic high-performance flip-flops. Flip-flop architecture named cross charge control flip flop (XCFF), which has considerable advantages over SDFF and HLFF in both power, area and speed. XCFF and DDFF are hybrid flip-flops which has a special property of reducing the large precharge capacitance and also makes the inert node to divide into two so that we

can drive the output network pull up and pull down by different node which makes a faster drive of the output. . In this paper, we propose a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFFELM). Both of them eliminate the drawbacks of XCFF.

2. EXISTING WORK

2.1 Static Flip-flop

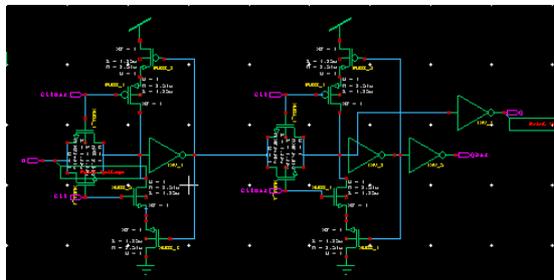


Fig1: Static Flip-flop

In order to overcome the problem of distributing several clock signals and avoid the serious problems caused by clock skew, a development of NORA-CMOS technique introduced True Single Phase Clock (TSPC) CMOS circuit technique TSPC flip-flops have the advantage of single clock distribution, small area for clock lines, high speed and no clock skew. The basic TSPC latches can be obtained in many ways to implement all essential sequential components. It show implementation of eight-transistor positive edge-triggered D flip-flop using split-output TSPC latches Although this structure seems to have smaller area than 9T TSPC flip-flop and less clocked transistors, it hasn't been used for simulations. The main reason is that there are some nodes in this structure which are not fully driven to VDD or GND.

2.2 Dynamic Flip-flop

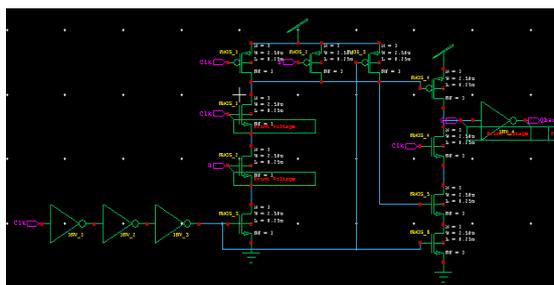


Fig2: Dynamic Flip-flop

This structure is basically a level sensitive latch which is clocked with an internally generated sharp pulse. This sharp pulse is generated at the positive edge of the clock using clock and delayed version of clock. Transistor level implementation of this flip-flop is shown in figure

2.3XCFF

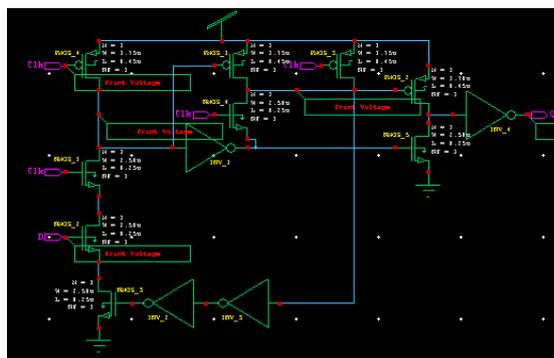


Fig3: Cross charge control flip flop XCFF

The large precharge-capacitance in a wide variety of designs results from the fact that both the output pull-up and the pull-down transistor are driven by this precharge node. These transistors being driving large output loads contribute to most of the capacitance at this node. This common drawback of many conventional designs was considered in the design of XCFF. It reduces the power dissipation by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors. Since only one of the two dynamic nodes is switched during one CLK cycle, the total power consumption is considerably reduced without any degradation in speed. Also XCFF has a comparatively lower CLK driving load. One of the major drawbacks of this design is the redundant precharge at node X2 and X1 for data patterns containing more 0 s and 1 s, respectively. In addition to the large hold time requirement resulting from the conditional shutoff mechanism, a low to high transition in the CLK when the data is held low can

cause charge sharing at node X1. This can trigger erroneous transition at the output unless the inverter pair INV1-2 is carefully skewed. This effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design

3. PROPOSED WORK

3.1 Dual Dynamic Hybrid Flip Flop

Dual Dynamic Hybrid Flip Flop (DDFF) which has extra inv4 occupies an additional area to flip flop and then it's requires more power. QB in the output is inverted by inv3, gets output as Q. So the output Q is again inverted and it's not required. One of the most drawback of DDFF is large area and more power. Inv4 which causes error when it's connected to QB.

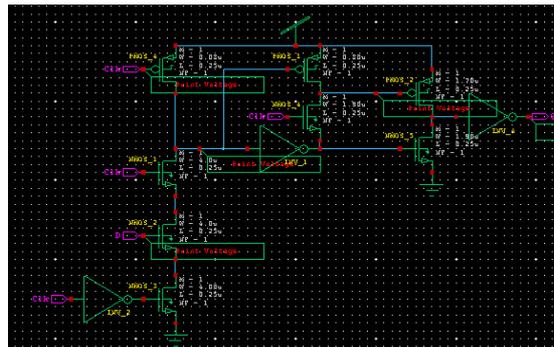


Fig4: DDFF

In the DDFF architecture, NodeX1 is pseudo-dynamic, with a weak inverter acting as a keeper, whereas, compared to the XCFF, in the new architecture node X2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF. The operation of the flip-flop can be divided into two phases: 1) the evaluation phase, when CLK is high, and 2) the pre charge phase, when CLK is low. The actual latching occurs during the 1-1 overlap of CLK and CLKB during the evaluation phase. If Dis high prior to this overlap period, node X1 is discharged through NM0-2. This switches the state of the cross coupled inverter pair INV1-2 causing node X1B to go high and output QB to discharge through NM4. The low level at the nodeX1 is retained by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs. Thus, nodeX2 is held high throughout the evaluation period by the pMOS transistorPM1. As the CLK falls low, the circuit enters the pre charge phase and node X1 is pulled high through PM0, switching the state of INV1-2. During this period node X2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node QB and maintain their voltage levels through INV3-4. If Dis zero prior to the overlap period, node X1 remains high and nodeX2 is pulled low throughNM3astheCLK goes high. Thus, node QB is charged high through PM2 andNM4 is held off. At the end of the evaluation phase, as the CLK falls low, node X1 remains high andX2 stores the charge dynamically. The architecture exhibits negative setup time since the short transparency period defined by the 1-1 overlap CLK of and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low. NodeX1 undergoes charge sharing when the CLK makes a low to high transition while Dis held low. This results in a momentary fall in voltage at nodeX1, but the inverter pair INV1-2 is skewed properly such that it has a switching threshold well below the worst case voltage drop at nodeX1 due to charge sharing. The timing diagram shows that node X2 retains the charge level during the pre charge phase when it is not driven by any transistor. Note that the temporary pull down at node X2 when sampling a "one" is due to the delay between X1 andX1B.

3.2 DDFF-ELM

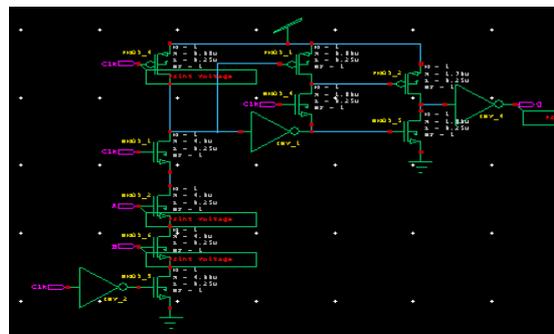


Fig5: DDFF-ELM

Dual dynamic node hybrid flip-flop with logic embedding capability (DDFF-ELM) transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed. The reason for this in clocking is the charge sharing, which becomes uncontrollable as the number of nMOS transistors in the stack increases. The same reason

makes XCFF also incapable of embedding complex logic functions. In order to get a clear picture of the charge sharing in XCFF, it was simulated with different embedded functions and the amount of worst case charge sharing was calculated

4. SIMULATION

These circuits are simulated in Tanner using TSMC025

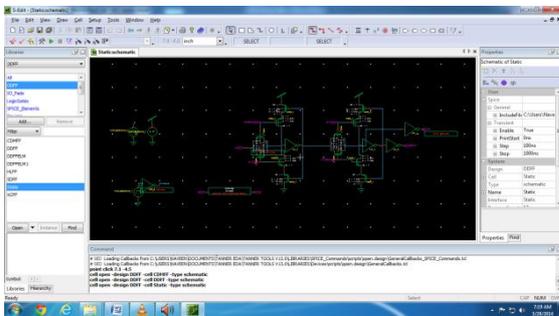


Fig6: Static Flip Flop design

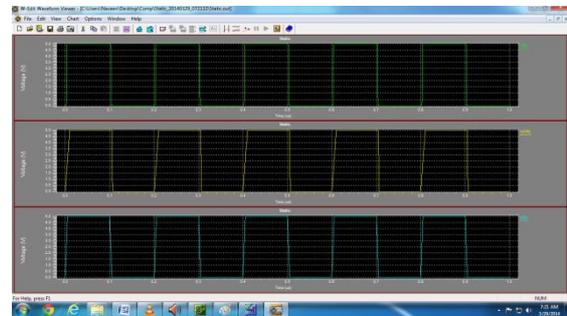


Fig7: Static Flip Flop Simulation

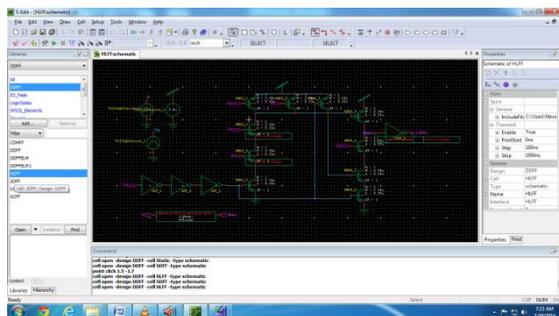


Fig8: HLFF Flip- Flop design

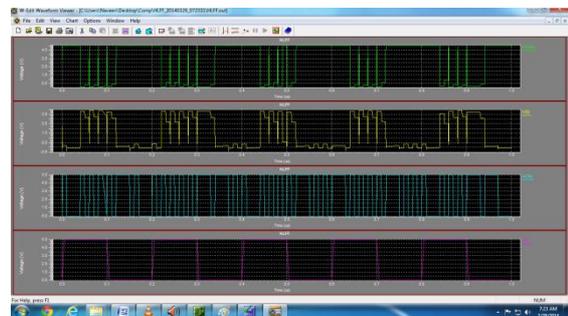


Fig9: HLFF Flip- Flop design simulation

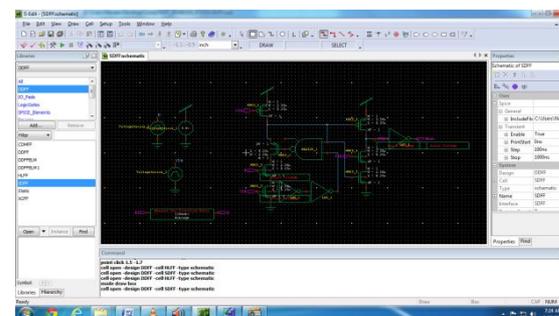


Fig10: SDFP Flip Flop design

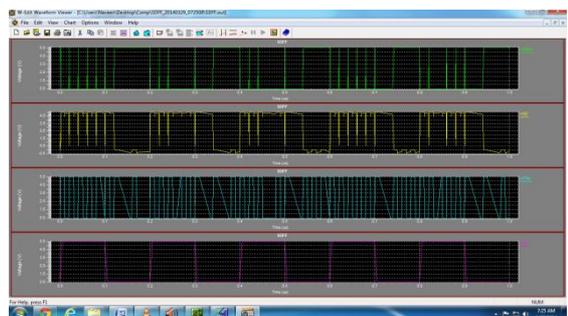


Fig11: SDFP Flip Flop design simulation

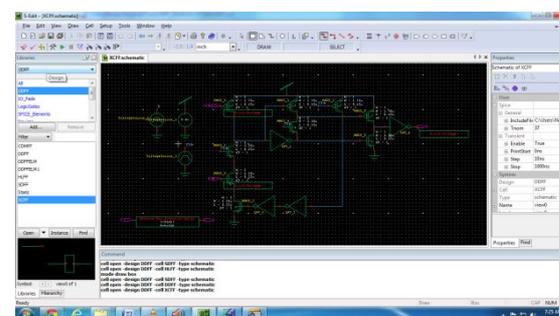


Fig12: XCFF Flip Flop design

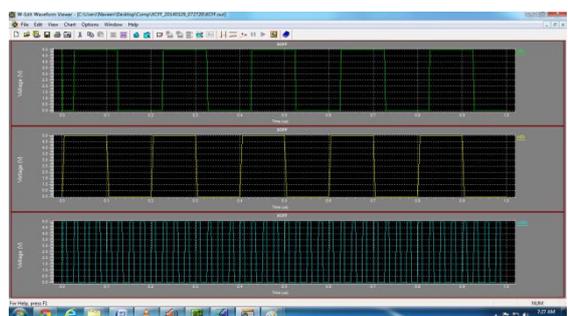


Fig13: XCFF Flip Flop design simulation

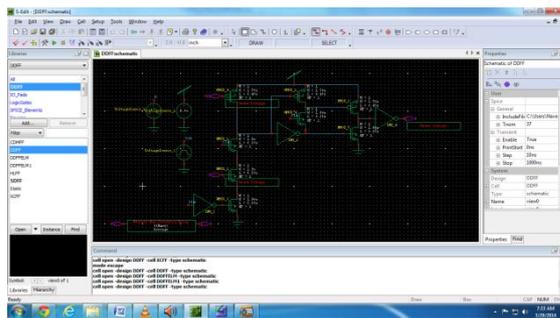


Fig14: DDFE Flip Flop design

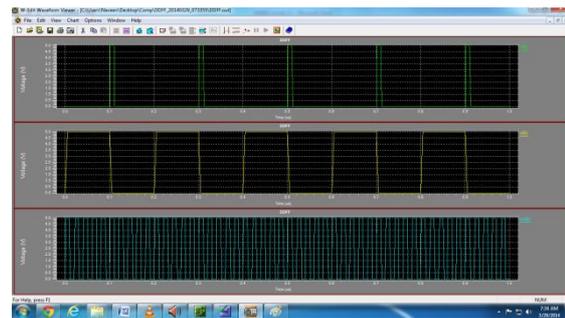


Fig15: DDFE Flip Flop design simulation

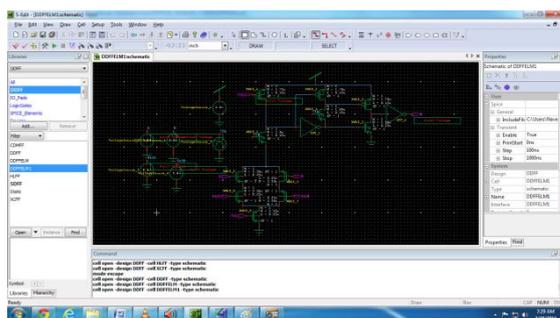


Fig16: DDFE Flip Flop with Mux as ELM

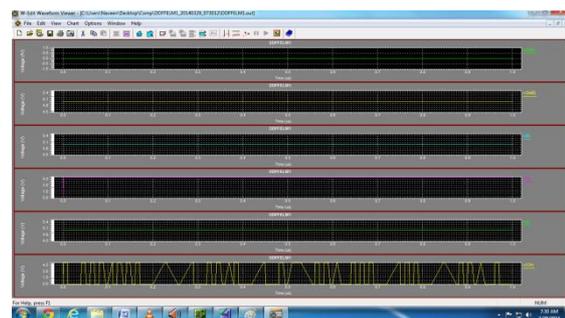


Fig17: DDFE Flip Flop with Mux as ELM simulation

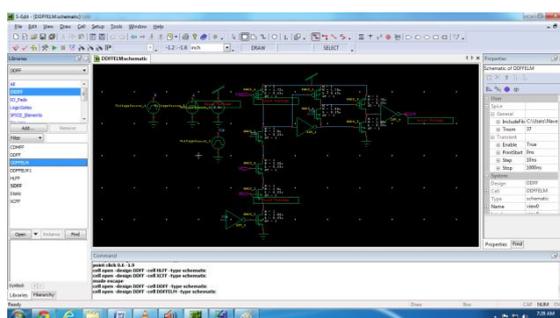


Fig18: DDFE Flip Flop design with NAND

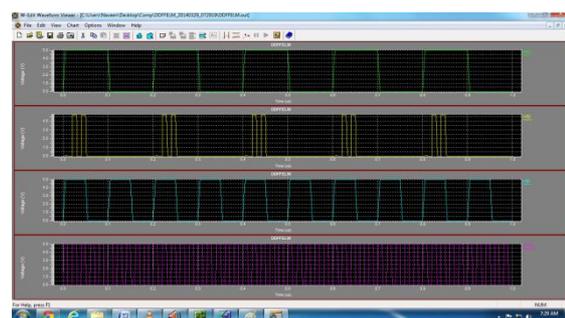


Fig19: DDFE Flip Flop design with NAND simulation

5. FUTURE SCOPE

In us future with the DDFE architecture we create various flip-flop applications that can embedded inside the flip-flop which will reduces the area and also power of the application

6. CONCLUSION

The results are compared with the existing Flip-Flops. The tabulation of performance comparison of existing and proposed methods is shown above. The active device has considerably increased when compared to the proposed methods. In this paper, a new low power DDFE and a novel DDFEELM were proposed. An analysis of the overlap period required to select proper pulse width was provided in order to make the design process simpler.

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