Implementation of Life Cycle Improvement for WMSN

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Abstract

This paper gives an overview of the life cycle improvement for wireless multimedia sensor networks. First, improvement methods are discussed. The main part of the paper is failure of various CMOS circuits as a result of Time Dependent Dielectric Breakdown (TDDB) and explores design techniques to increase the mean time to failure (MTTF) of large-scale circuits. Time Dependent Dielectric Breakdown is a phenomenon where the oxide underneath the gate degrades as a result of the electric field in the material. Currently, there are few well documented design techniques that can increase lifetime, but with a tool chain called the MTTF Analyzing Program, or MAP, the circuits were tested under various conditions in order to identify weak links, discover relationships, and reiterate on my design and see improvements and effects, followed by the other method Electro Migration (EM). The results of these process developments and the mechanisms of EM improvement will be discussed in this paper.

Keywords: TDDB, Failure Mechanisms, Electro Migration, Metal Barrier and Seed Optimization

1. INTRODUCTION

Time Dependent Dielectric Breakdown: With the scaling down process of microcircuits, the effects of Time Dependant Dielectric Breakdown are becoming increasingly severe. Time Dependent Dielectric Breakdown (TDDB), the phenomena where the oxide underneath the gate material of a MOSFET degrades resulting in a short circuit. As technology scales down, the oxide becomes thinner and more fragile allowing the affects of TDDB to become more severe. In order to combat TDDB, engineers and scientists have used different dielectric materials and have also designed circuits for lower power consumption and a lower rail voltage. However, there have been few to no circuit design solutions.

Electro Migration: Electro Migration (EM) reliability has become a growing concern for Cu interconnects in advanced technology nodes. The interface between the dielectric diffusion barrier (SiCN) and copper, metal barrier quality and metallization homogeneity are all critical to EM performance. Our EM enhancement investigation has focused on improving the SiCN/Cu interface, metal barrier quality and metallization homogeneity while mitigating the process integration risk and cost. Multiple processes developed at Novellus have demonstrated significant EM improvement without compromising stress migration or dielectric reliability.

2. TIME DEPENDENT DIELECTRIC BREAKDOWN

Time Dependent Dielectric Breakdown is a phenomenon where the oxide underneath the gate degrades. As the name implies, it is the breakdown of a dielectric over time. There are other ways a dielectric can breakdown but in a digital system, the only variables are operating frequency, voltage supply, MOSFET characteristics (such as gate area or dielectric material), temperature, and time.

As the gate-oxide is scaled down, breakdown of the oxide and oxide reliability becomes more of a concern. Higher fields in the oxide increase the tunneling of carriers from the channel into the oxide. These carriers slowly degrade the quality of the oxide and over time, leads to failure of the oxide [1]. Once a dielectric breaks down, current is able to flow more easily through the gate into the drain/source of a P/NMOSFET completely destroying functionality. Evidence of TDDB are changes in the threshold voltages and the drain currents as well as a great increase in current through the dielectric [2] and ultimately the gate as shown in Figure 1.

![Figure 1 Relationship between TDDB and Leakage Current](image-url)
3. FAILURE MECHANISMS / TDDB EFFECTS

3.1. Time Dependent Dielectric Breakdown: Quantum Tunneling

There are many hypotheses for why TDDB occurs. Many models describe what occurs in the dielectric material over time and each model consequently has a mathematical model that can predict the expected failure of a device. There has been much speculation for the last 50 years as to which model correctly predicts the failure time. But there is general consensus that the electric field through the dielectric material is the direct cause of TDDB. This relationship is shown in Figure 2.

![Figure 2](image)

**Figure 2 Relationships between TDDB and the Electric Field**

The simple explanation is that the electric field breaks down the oxide, but electric fields could be the cause of more specific phenomena, such as band-to-band impact ionization, hole trapping near the injecting interface, and electron trapping [2], but it is accepted that it is caused by charge that remains in the oxide [3]. Ideally charge should not pass through the oxide, but thinner oxides and stronger electric fields make this possible. Strong electric fields lead to quantum tunneling effects such as Fowler-Nordeim Tunneling, Direct Tunneling, and Trap Assisted Tunneling [4].

Fowler-Nordeim Tunneling is a quantum mechanical process where electrons can penetrate through the oxide barrier into the conduction band of the oxide [4]. Tunneling is exponentially dependent on voltage. Direct Tunneling is another process where electrons penetrate through the gate directly to the channel [4]. In this process, tunneling increases exponentially with the decrease of oxide thickness. Trap Assisted Tunneling is again another important process where electrons go through the oxide into traps, which are empty bonding sites within the oxide, and then proceed into the silicon.

![Figure 3](image)

**Figure 3 Various Quantum Tunneling Illustrations [4]**

There are at least five (5) oxide breakdown models currently used by reliability engineers: the Bandgap Ionization Model, the Classic Anode Hole Injection (1/E) Model, the Hydrogen Release Model, the Thermochemical (E) Model [4], and a combination of the Charge-to-Breakdown (QBD) Hypothesis and the Poole-Frenkel (PF) Conduction (√E) Mechanism [5]. The important models to consider are the Classic Anode Hole Injection Model, the Thermochemical Model, and the Poole-Frenkel Conduction Mechanism because they have commonly used mathematical models to predict time failure and have been thoroughly tested to provide some accurate results.

3.2. Time Dependent Dielectric Breakdown: The E, 1/E, and The √E Models

According to the Thermochemical (E) Model, the electric field applied to the gate, creates traps within the oxide. This process is further aggravated by temperature. The mathematical equation for the mean time to failure, \( \tau \), to model this phenomenon is:

\[
\tau = A \exp\left(\frac{E_g}{kT}\right) \exp\left(-\frac{\gamma E_f}{kT}\right)
\]

(1)
where $A$ is a constant, $E_A$ is the activation energy, $k$ is Boltzmann’s constant, $T$ is temperature, $\gamma$ is the field acceleration factor, and $E_f$ is the electric field strength in the oxide [4] [6]. It is usually referred to as the E model because of its $E$ dependence as can be seen in the second exponential.

Classic Anode Hole injection (1/$E$) Model predicts that some electrons entering the anode of a transistor will have enough energy to create a “hot” hole which can tunnel back into the oxide. This can happen at either high or low energies, but it can be observed most clearly with electrons with very high energy [4]. The mathematical equation for the mean time to failure to model this phenomenon is:

$$\tau = \frac{A \exp\left(\frac{E_a}{kT}\right) \exp\left(-\frac{\gamma}{E_f}\right)}{E_f}$$  \hspace{1cm} (2)

where again, $A$, $E_A$, $T$, and $\gamma$ is the same as in equation (1) above. As with the E model, this model is called the 1/$E$ model because of its 1/$E$ dependence in the second exponential [7].

The charge to breakdown hypothesis and the Poole-Frenkel Leakage Mechanism ($\sqrt{E}$) are the basis for the last major model. The charge to breakdown hypothesis states that once a critical charge has been forced through the dielectric, the dielectric will break down. Also, the Poole-Frenkel Leakage Mechanism predicts that leakage current interacts with the dielectric which leads to degradation [5]. The corresponding equation is:

$$\tau = \frac{Q_{BD}}{E_f} \exp\left(\frac{q[\Phi_B - \frac{qE_f}{\pi\varepsilon_0\varepsilon_{r}}]}{kT}\right)$$  \hspace{1cm} (3)

where $E_f$ is the electric field like the previous two models, and $Q_{BD}$ is the critical charge or the breakdown charge, $\Phi_B$ is the trap depth, $q$ is the elementary charge, $\varepsilon_0$ is permeability in a vacuum, and $\varepsilon_{r}$ is permeability in the dielectric [5]. Again, the square root $E$ dependence can be seen.

To combat the effects of TDDB, different methods were employed. Thicker oxides have been used, but as technology continues to scale down, as does the thickness of the dielectrics and with each new VLSI generation, TDDB becomes a greater concern.

![Figure 4 TDDB vs. Dielectric Constant, as well as VLSI Generations][1]

There are numerous papers published about different chemical compounds that could be used as a replacement for Silicon dioxide and some show promising results [1]. Such alternate oxides are called high-k dielectrics. These oxides have a greater dielectric constant so that the same gate capacitance can be obtained with a thinner oxide. The oxides tested are Al2O3, ZrO2, and TiO2 [1]. A graph showing different compounds and different oxide thicknesses and the effect on MTTF is shown in Figure 2.2.3.

Another attempt is lowering the power supply voltage which serves two purposes. In addition to reducing the power consumption of a circuit, it has been proved that lowering $V_{dd}$ of a circuit can increase its lifespan [8]. Gate area also has an effect on TDDB. It has been proven mathematically as well as through experimentation, and as expected, pulse stressed circuits lasted longer than DC stressed circuits [7].
4. ELECTRO MIGRATION

4.1. Metal Barrier and Seed Optimization

The metal microstructure and the interface along the liner and cap layer are both critical to interconnect reliability [9]. Vias with high aspect ratios or "reentrant" profiles may lead to poor metal barrier coverage and the premature failure of the interconnect. Degradation of EM was observed when a non-uniform metal barrier process was used [10]. A barrier-first approach with re-sputter was developed to provide good step coverage for the via bottom corner and the "reentrant" area of the feature [11]. Additionally, with thinner barriers film morphology and density become increasingly important to maintaining barrier integrity and ensuring a good interface with the copper seed. HCM IONX Ta(N) uses a high density plasma and optimal ion energy with Hollow Cathode Magnetron (HCM) PVD technology to optimize the metal barrier microstructure. A high density metal barrier with smooth morphology and improved dielectric reliability was demonstrated in the experiment [12, 13]. Conformal copper seed step coverage is also essential to provide homogeneous metallization for the small features. RF copper deposition with respatter technology developed on the INOVA HCM source produces near-conformal copper step coverage. A combination of the HCM IONX Ta(N) and RF copper source leads to substantial improvements in Cu gapfill capability and EM performance. Significant improvements in both time-to-failure and sigma of distribution (Figure 5) are observed with the high density barrier and RF copper seed process [14].

![Figure 5](image)

**Figure 5** Effect of barrier/seed on EM. Significant improvement in both TTF and distribution is observed with the IONX PVD relative to conventional HCM PVD.

**PECVD self-aligned barrier.** The interface between SiCN and copper has been shown to be the main path for copper diffusion, and the weakest link in resisting EM failure. Many approaches have been explored to improve this SiCN/copper interface. Selective metal caps, such as CoWP, have demonstrated significant EM improvement and received much interest. The implementation of a selective metal CoWP cap, however, is expensive and difficult due to limitations in achieving good selectivity to deposition over copper versus dielectric surfaces, and may lead to degraded dielectric reliability. A self-aligned barrier, on the other hand, has good deposition selectivity and may be implemented through a slight modification to the SiCN unit process without degrading the electrical isolation characteristics of the intra/inter-metal dielectric layers. The PECVD self-aligned barrier (PSAB) has attracted much attention recently due to its high selectivity, low cost of implementation and benefits to interconnect reliability [15, 16]. The typical process steps in forming a PSAB have been described previously [17]. High selectivity of the PSAB process arises through the natural differences in reactivity and reaction products of the gaseous constituents with the Cu and dielectric surfaces. In the case of Si-based PSAB, SiH₄ exhibits thermally-activated reaction with Cu, but the reaction on the dielectric surface results in the formation of an insulating film. Similarly, Ge reacts rapidly with Cu as shown in the SIMS analysis, but electrical testing shows no indication of Ge reaction with various dielectric films [17].

Significant improvement in mean-time-to-failure (MTTF) for the downstream EM test is noted with the integrated Ge-PSAB scheme as compared to the control. Details of the mechanism for EM improvement are still under investigation. Previously, we reported TDDB and EM improvements associated with improved adhesion of the low-k SiC to both Cu and low-k dielectric, enabling better encapsulation of the Cu inside the trench [16]. In this work, adhesion energy measurements for both the control and Ge-PSAB/Cu interfaces were measured to be high and similar. The distribution of the Ge inside the Cu shows a higher concentration of Ge near the Cu-SiCN interface [17]. The thin layers of CuGe₆ may aid in retarding the growth of the nascent defects (voids) within the interconnect structure. In addition, the cladding layers around the Cu surface create a shunt layer around the lower resistivity conducting metal, diverting the
current away from the weaker interface. Diffusion of Cu with the electron wind would disturb the metallurgical equilibrium of the CuGe/Cu structure due to increases in the concentration of Ge in Cu-depleted areas near the interface. This creates a net force proportional to the concentration gradient, opposing electromigration [17]. The above-mentioned mechanisms would lead to void growth delay without changing the failure mode. This is consistent with our investigation, where the EM activation energy of the Ge-PSAB is similar to that of reference SiCN, but the EM time-to-failure is much longer.

Alloy seed. Metal alloying has been widely used in semiconductor processes since the Al-interconnect era. Multiple Cu-alloying elements and approaches were investigated to improve reliability [18]. Cu-Al alloys have received much attention. It was observed that alloying Cu with Al increases the incubation time for void growth and decreases the Cu drift velocity [19]. PVD processing has been the preferred approach for Cu alloying due to the readily-available alloy targets, lower cost and easier process control. The alloying of Cu with Al, however, increases the Cu interconnect resistance and thus degrades RC delay. Our investigation of Cu-Al alloy seed integration focused on the tradeoff between increased resistance and improved reliability, with the goal of minimizing the RC delay degradation while maintaining the benefits of Cu-Al alloy seed. Through this process development and integration optimization, a new alloy seed process was developed.

The downstream package electro migration test results suggest clear correlation between time-to-failure (TTF) and Al doping concentration for conventional alloy seed process (Figure 6). Significant EM improvement can be achieved with the Cu-Al alloy approach, but it leads to a large increase in RC delay. A measure of the tradeoff between EM improvement and an increase in RC delay, defined as the "EM improvement efficiency", was recently proposed by S. Yokogawa et al. [20]. Here it was concluded that with conventional Cu-Al alloy seed -- while significantly improving EM lifetime the EM improvement efficiency was not as high as with the CoWP metal cap approach.

A new alloy seed approach was developed with the HCM PVD process to enhance the EM improvement efficiency without compromising dielectric reliability and stress migration performance [11]. The EM improvement with alloy seed as a function of the normalized line resistance is plotted in Figure 4. Consistently higher EM improvement efficiency, defined as the slope of the plot in Fig. 7, is demonstrated with the new HCM alloy seed process. This process allows the use of a PVD process based on HCM technology to provide EM improvement for advanced technology nodes.
The improvement in EM with a Cu-Al alloy is attributed to a slower Cu drift velocity and a lower void growth rate [20]. SIMS depth profile analysis indicates Al diffuses through Cu and accumulates at the SiCN/Cu interface upon thermal anneal [13]. It is hypothesized that the Al getters the residual oxygen at the SiCN/Cu interface, driving the segregation at the SiCN/Cu interface and improving electromigration. The improvement of the SiCN/Cu interface, along with slower Cu drift and reduced Cu void growth rate, greatly enhances electromigration performance with use of the Cu-Al seed. While the mechanisms are still under investigation, we believe that this new HCM alloy seed process allows the formation of a homogeneous Cu microstructure inside small features and strengthens the Cu/SiCN interface, leading to improved EM resistance.

Ti(N) metal barrier. The need for reliability improvement also led us to investigate alternative metallization approaches. A Ti(N) metal barrier was once considered to be inappropriate for Cu metallization due to potential F attack from fluorine-doped silicate (FSG). However, as carbon-doped oxide (CDO) replaces FSG for interconnect dielectrics, interest in Ti(N) barrier as the metal barrier has returned. The interfaces between the Cu/Ti(N) metal barrier, Ti(N)/dielectric and SiCN/Cu are all critical to the reliability performance. Our dewetting investigation result suggests poor Cu wetting behavior on TiN, but excellent Cu wetting on Ti. However, Ti is known to diffuse into Cu, raising Cu resistivity, and is not able to provide the needed barrier properties. Here, a composite Ti/Ti(N)/Ti layer is proposed to address both Cu/Ti(N) interface and Cu diffusion barrier concerns [21].

No RC delay is observed with an optimal Ti(N) process, even though Ti diffusion into Cu is detected. This result can be attributed to accelerated Cu grain growth when Ti(N) is used as the metal barrier. Larger Cu grain alleviates the Cu resistivity increase due to Ti doping. SIMS profile analysis indicates Ti aggregation at the SiCN/Cu interface, similar to our observation with Cu-Al alloy seed. Ti also acts as an oxygen getter at the interface, and reinforces the SiCN/Cu interface. This mechanism is further supported by the higher adhesion energy and detection of TiOx at the SiCN/Cu interface. Significant EM improvement is observed with a Ti(N) metal barrier, as shown in Figure 8.

**Figure 8** Downstream EM performance for Ta(N) and Ti(N) based metal barrier. 10x longer EM TTF is demonstrated with Ti(N) based metal barrier.

Process synergy. Multiple paths were explored for improvement of EM. A PSAB approach enhances the SiCN/Cu interface with the formation of a shunt layer near the SiCN/Cu interface, prolonging the voids growth within the interconnect structure. An alloy seed approach improves the EM performance through different mechanisms. The capability to combine various low cost, low risk reliability improvement approaches to meet the increasing reliability challenges provides greater benefits than employing radical process changes.

5. CONCLUSION

Time Dependent Dielectric Breakdown has the potential to be a large trouble if not addressed, particularly with the scaling down of technology. There has to be circuit design solutions that exist to combat this increasing problem. This paper presented a tool chain with MAP at its core that was used to calculate mean time to failure for a given circuit. When completed, the tool chain was used to analyze a variety of circuits to simulate the wear and tear of real life circuit under stress. Multiple paths to improve EM performance are demonstrated. Optimization of the metal barrier and copper seed processes provides reliability improvement through a high quality metal barrier and homogeneous copper metallization. Further EM enhancement can be achieved through a novel copper alloy seed approach, which provides higher EM Improvement Efficiency over conventional Cu-Al alloy seed.

References


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